ELECTROMAGNETIC ANALYSIS AND DESIGN OF DIVIDERS AND COUPLERS AT *X*-BAND

X-BANT BÖLÜCÜ VE BAĞLAŞTIRICILARIN ELEKTROMANYETİK ANALİZİ VE TASARIMI

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Submitted to

Graduate School of Science and Engineering of Hacettepe University

as a Partial Fulfillment to the Requirements

for be Award of the Degree of Master of Science

in Electrical and Electronics Engineering

2019

The work titled "**Electromagnetic analysis and design of dividers and couplers at *X*-band**" by **HAMDİ ARMAĞAN GÜRDAL** has been approved as a thesis for the Degree of **MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONICS ENGINEERING** by the Examining Committee Members mentioned below.

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Hamdi Armağan Gürdal

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ÖĞRENCİNİN ADI-SOYADI

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ABSTRACT

ELECTROMAGNETIC ANALYSIS AND DESIGN OF DIVIDERS AND COUPLERS AT *X*-BAND

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June 2019, 71 pages

Power divider and combiner structures are the necessary and crucial passive components in order to reach high power levels for the microwave applications. The improvements in the RF/Microwave systems in the past decades have led to increasing demand for the compact, high performance power divider/combiners.

In this thesis, four-way offset power divider/combiner, two-way ring power divider/combiner, three-way phase shifted Wilkinson power divider/combiner and four-way corporate power divider are designed at 8-12 GHz frequency band by using miniaturization techniques. Their analytical solutions are presented, and design procedures are explained using Advance Design System (ADS) software environment. These divider and combiner structures are fabricated using Bilkent University Nanotechnology Research Center (NANOTAM)'s Gallium Nitride (GaN) on Silicon Carbide (SiC) process. Details of the fabrication steps are demonstrated. On-wafer measurements of the designed divider and combiner structures are performed in NANOTAM laboratories are presented. Measurement

and simulation results for insertion losses, input and output losses and isolations of the output ports are investigated for each power divider/combiner structures. Comparison of the measurement and simulation results are examined in detail.

Keywords: *X*-band, power divider, scattering parameters, coplanar waveguide (CPW), microstrip (MS), miniaturization.

ÖZET

X-BANT BÖLÜCÜ VE BAĞLAŞTIRICILARIN ELEKTROMANYETİK ANALİZİ VE TASARIMI

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Haziran 2019, 71 sayfa

Güç bölücü ve birleştirici yapılar, mikrodalga uygulamalarında yüksek düzeyde güçlere ulaşabilmek için gerekli ve kritik pasif elementlerdir. Son yıllardaki RF/Mikrodalga sistemlerindeki gelişmeler, yüksek kaliteli, yüksek performanslı güç ayırıcı/birleştiricilere olan talebin artmasına neden olmuştur.

Bu tez çalışmasında, dört yönlü ofset güç bölücü/birleştirici, iki yönlü halka güç bölücü/birleştirici, üç yönlü faz kaydırmalı Wilkinson güç bölücü/birleştirici ve dört yönlü birleşmiş güç bölücü, minyatürleştirme teknikleri kullanılarak, 8-12 GHz frekans bandında dizayn edilmiştir. Analitik çözümleri ve tasarım prosedürleri Advance Design System (ADS) yazılımı kullanılarak incelenmiştir. Bu bölücü ve birleştirici yapılar Bilkent Üniversitesi Nanoteknoloji Araştırma Merkez'inin (NANOTAM) Silisyum Karbür (SiC) tabanlı Galyum Nitrür (GaN) prosesi kullanılarak üretilmiştir. Fabrikasyon detayları adım adım gösterilmiştir. Tasarlanan bölücü ve birleştirici yapılar, NANOTAM laboratuvarlarında ölçülmüştür. Her güç bölücü/birleştirici yapı için ekleme kayıplarının, giriş ve çıkış geri dönüş kayıplarının ve çıkış portlarının yalıtımının ölçüm ve simülasyon

sonuçları incelenmiştir. Ölçüm ve simülasyon sonuçlarının karşılaştırılması detaylı olarak sunulmuştur.

Anahtar Kelimeler: *X*-Bant, güç bölücü, saçılma parametreleri, eş düzlemli dalga kılavuzu (CPW), mikroşerit (MS), minyatürleştirme.

Acknowledgement

First and foremost, I would like to thank my supervisor Prof. Dr. Birsen Saka for her valuable support, guidance and instructive comments in this thesis study. It was an honor for me to work on this thesis study with her. I also would like to extend my thanks to Prof. Dr. Çiğdem Seçkin Gürel, Dr. Dinçer Gökçen, Prof. Dr. Ekmel Ozbay and Prof. Dr. Özlem Özgün for being my jury members.

I would also like to thank Prof. Dr. Ekmel Özbay for supporting and encouraging me in this thesis work. I would like to thank fabrication team in NANOTAM for producing good SiC wafers.

Special thanks to my senior Ömer Cengiz in Nanotam for guiding design stages and giving advices. I would also like to thank my colleagues from Nanotam; Büşra Çankaya, Muhammet Kavuştu and Batuhan Sütbaş for charitable help. I would also like to special thank Ulaş Özipek for his discussions and suggestions at every time. Without him, I may not have ended in the finish line.

I would also like to thank Oğuz Yeğin for supporting and assisting me throughout my graduate education.

My special thanks belong to my family; Ayşe Gürdal, İbrahim Gürdal and Arda Gürdal for helping and assisting me at every stage in my life.

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1. INTRODUCTION

Power dividers and couplers are passive components which are used very frequently in the microwave applications. Multifarious non-planar power dividers and waveguide couplers were invented and designed at the Massachusetts Institute of Technology (MIT) Radiation laboratory in the 1940s [1]. In the middle of 1950s, these couplers and power dividers are redesigned by using planar structures technologies such as striplines and microstrip lines [2]. Well known Power dividers and couplers such as branch line coupler, Wilkinson Power Divider (WPD) [3], Gysel power divider [4] and coupled line directional coupler were invented alongside the increasingly widespread usage of stripline and microstrip line technologies at these years.

The developments in the RF/Microwave systems in the past decades have led to increasing demand for the high quality, high performance power divider/combiners. As the requirement of power density in the wireless communication technologies increase significantly, capability of single-solid state devices become insufficient to reach high enough power levels. Therefore, power dividers and combiners are used to reach high output powers by dividing, amplifying and then combining the RF signals. This way, devices or amplifier blocks remain operating at lower powers while the total output power reaches higher levels. Also, RF stress which is caused by high power on active devices and passive components is relaxed.

Power dividers split incoming RF signal into 2 or more output signal. Generic block diagram of the power divider and combiner is given in Figure 1.1. Dividing/combining ratio of the power dividers/combiners or number of the dividing/combining incoming signal may differ according to design requirements.

Power dividers/combiners are mostly used to obtain higher output power for the Monolithic Microwave Integrated Circuits (MMICs). Combining number of amplifiers or multiple transistors within a single amplifier with the power divider/combiner circuits, output power capabilities and/or linearity of the circuits are enhanced [5]. Expected qualities from an ideal power divider/combiner are low insertion loss [6], [7], high isolation [8], [9] and a broad

operation bandwidth [10], [11]. In addition, due to the high cost in integrated circuits, area - performance of the power dividers/combiners is also significant for the designers [12], [13].

Developments on GaN technology increase speedily in the 90s because of the advance of the GaN HEMTs. GaN HEMTs are convenient for the high-power microwave applications because of the fact that they have wide bandgap and high electron mobility. In addition, GaN technology provides operating at the higher temperatures than other wide-bandgap technologies. GaN on Sic technology has also higher thermal conductivity than GaAs technology.

In thesis work, four-way offset power divider/combiner, two-way ring power combiner /divider, three-way phase shifted WPD and corporate power combiner/divider with four-way structures are presented. Their analytical solutions, design procedures and measurements are discussed. These divider/combiner structures are fabricated at Bilkent University Nanotechnology Research Center (NANOTAM)'s Gallium Nitride (GaN) on Silicon Carbide (SiC) microfabrication process.

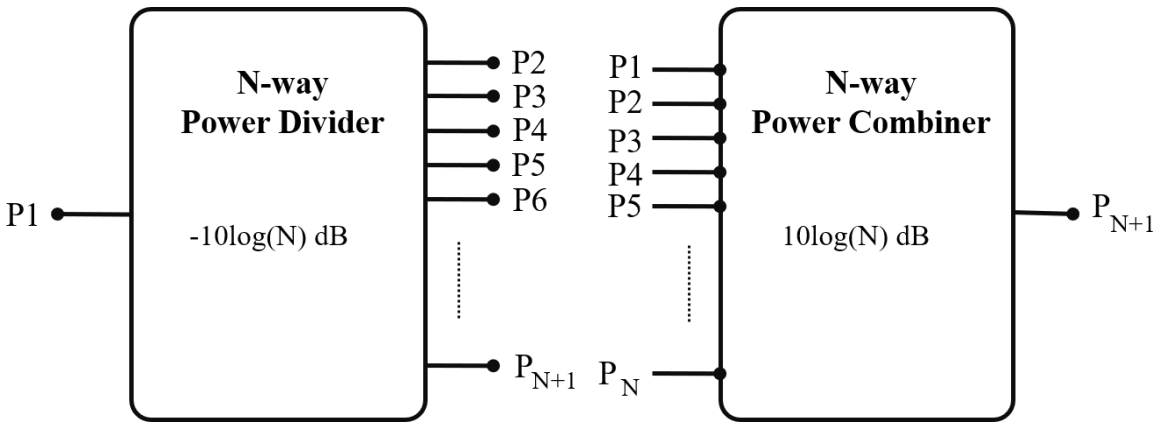


Figure 1.1 Simple block Diagram of N-way power (a) Divider (b) Combiner

In appendix I, brief information on the NANOTAM GaN on SiC process that are relevant for the passive component fabrication is given. Process steps involved in the fabrication of passive structures are explained with the help of figures and Scanning Electron Microscope (SEM) images.

In chapter 2, simulation and layout design environment are demonstrated. Optimization of the EM substrate stack using Advance Design System (ADS) for the simulations of divider/combiner structures are explained. Passive element photomasks prepared for EM model development, consisting of various CPW and MS circuit elements are presented. Test setups and infrastructure used for two port, three port and four port on-wafer S-parameter measurement are shown.

In chapter 3, four different power divider/combiner structures which are four-way offset power divider/combiner, two-way ring power combiner/divider three-way phase shifted WPD and corporate power divider with four-way are explained in detail. Their analytical solutions, synthesis techniques, circuit and layout designs are discussed. Finally, EM simulation results of finished designs and measurements of the fabricated structures are presented.

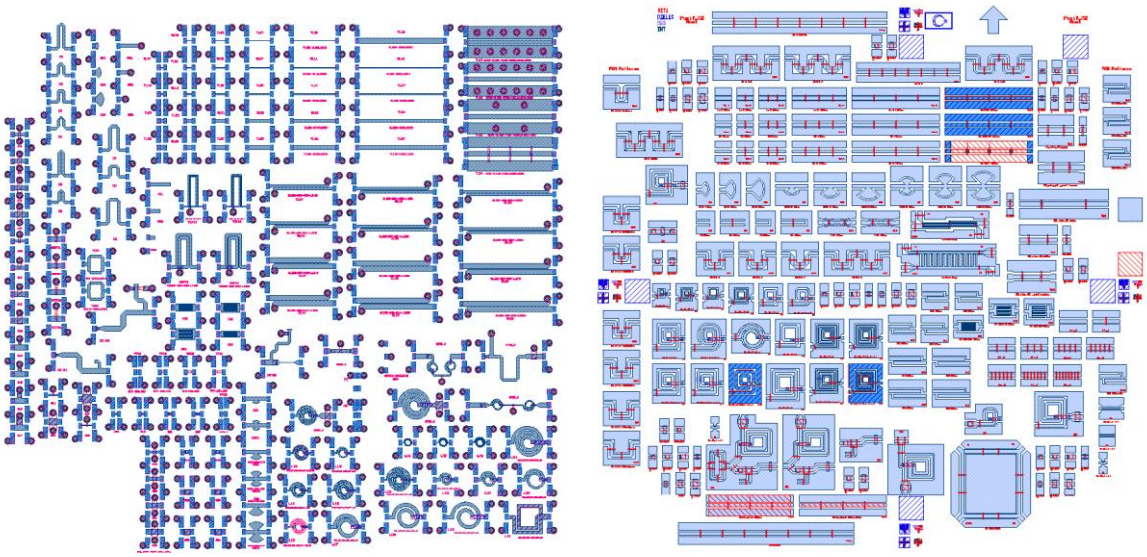
In conclusion chapter, results are summarized, comparisons of the designed and fabricated power divider/combiner structures are illustrated. Future work and possible improvements are discussed.

2. SIMULATION AND MEASUREMENT

In thesis chapter, simulation parameters, substrate details and EM model library is demonstrated. Small signal measurements with 2-port, 3-port and 4-port are explained with figures and images.

2.1. ADS Simulation Parameters

Advance Design System (ADS) is a commonly used tool to design power divider/combining structures in order to perform 3D EM simulation. First of all, two type masks that consist of wide various CoPlanar Waveguide (CPW) and MicroStrip (MS) series capacitors, shunt capacitors, inductors, resistors, open and short stubs, radial stubs, coupled lines, transmission lines and some passive structures are designed and fabricated at NANOTAM. Layout views of the masks are given in Figure 2.1.



(a) (b)

Figure 2.1 Layout views of the (a) CPW masks and (b) MS masks

Small-signal measurements are performed for these passive components. Measurement results and simulation results for different passive components are tried to fix by tuning substrate parameters. Finally, optimized substrate is created as shown in Figure 2.2.

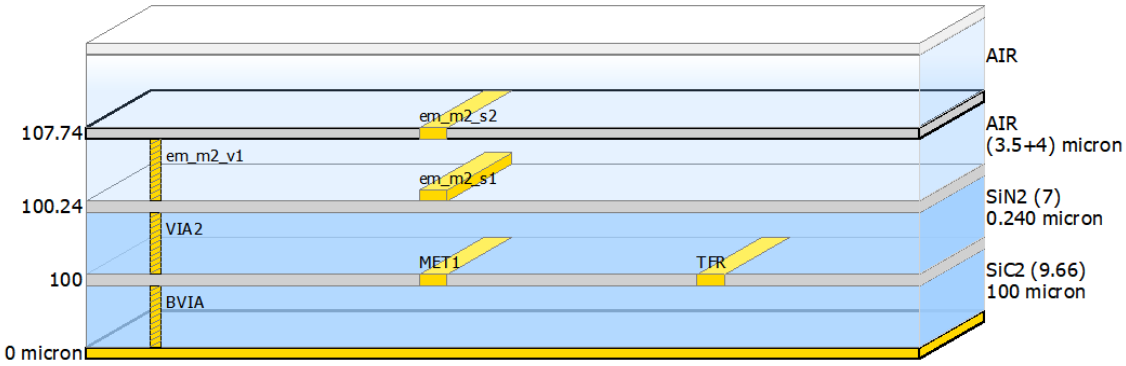


Figure 2.2 Cross-sectional view of substrate used in 3D EM simulations

MET1 layer is the first metal, TFR layer is the resistor, em_m2_s1 layer is the interconnect metal and em_m2_s2 layer is also interconnect metal for the air-bridge structure. For the fast simulation, some materials are defined as sheet metal. As shown in Figure 2.2 MET1, TFR and em_m2_s2 are sheet metal which means their thicknesses are 0 um at the simulation. Thickness of em_m2_s1 layer is given as 4um. Air-bridge space is defined as 3.5um. In addition, material properties are defined as dielectric constant of SiC2 and SiN2 are 9.66 and 7 with 0.03 and 0.001 loss tangent (TanD), respectively. Conductivities of the metal-1 is determined as 3.4e7 Siemens/m. Conductivities of the metal-2 layers are 3.7e7 Siemens/m. Back side metal is determined as perfect conductor. Resistance of the TFR layer is defined as 15ohm/square or 30ohm/square related to fabrication process. One of the 3D EM view of designed passive structure is given in Figure 2.3.

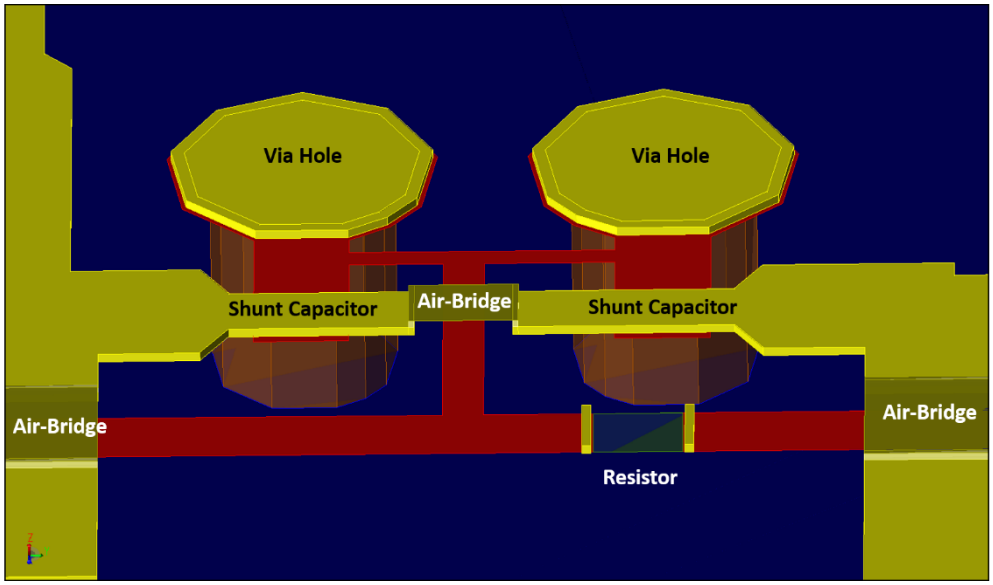


Figure 2.3 Momentum 3D preview of example passive structure

2.2. Measurement Setup

Small-signal measurements of the presented power divider/combiner structures are performed in RF laboratory at NANOTAM. Photography of the small-signal measurement setup is given in Figure 2.4.

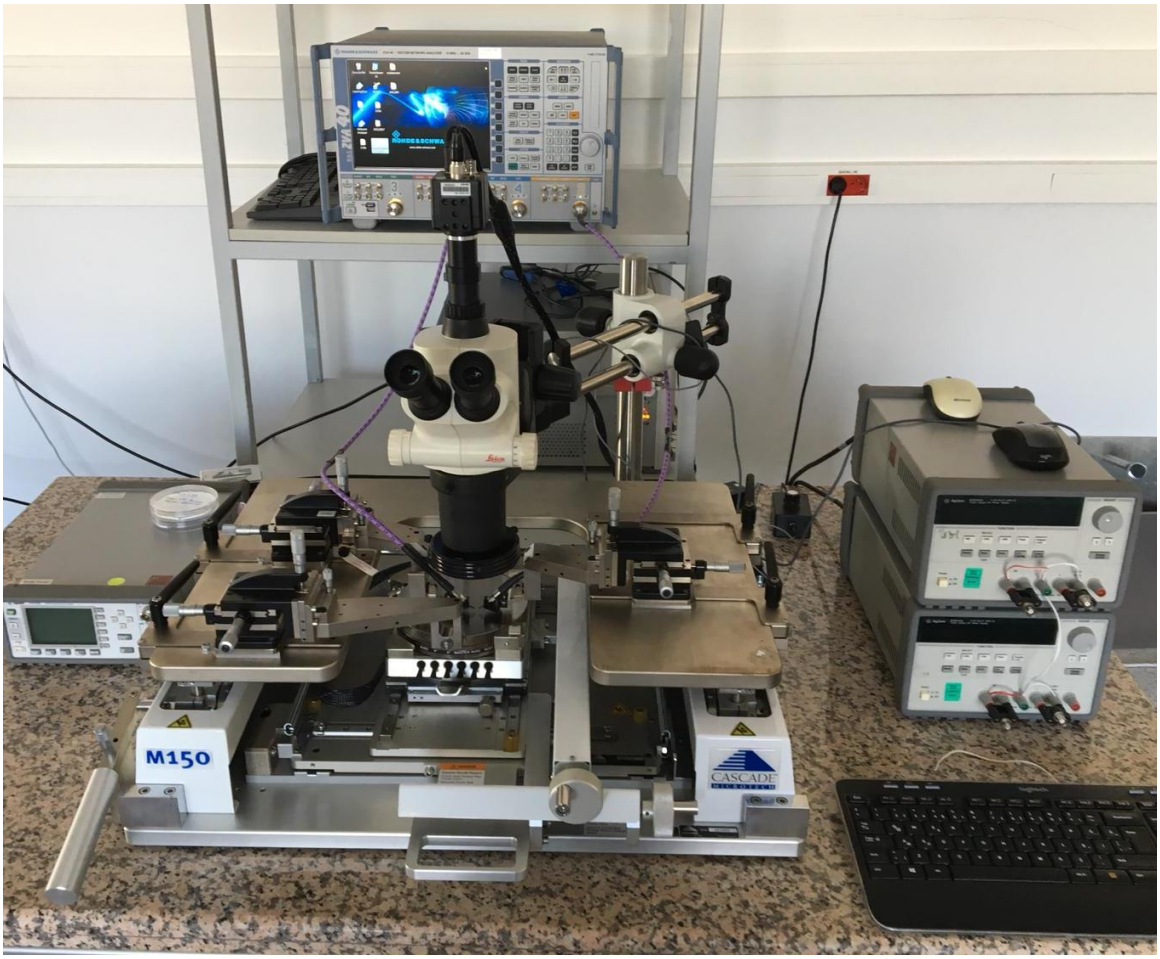


Figure 2.4 Photography of the small-signal measurement setup

Rohde & Schwarz ZVA40 Vector Network Analyzer (VNA) that is given in Figure 2.5 is used in order to perform three-port and four-port small signal measurements. Frequency range is 10MHz to 40GHz and number of ports is four. Detailed information about ZVA40 is given in [16].

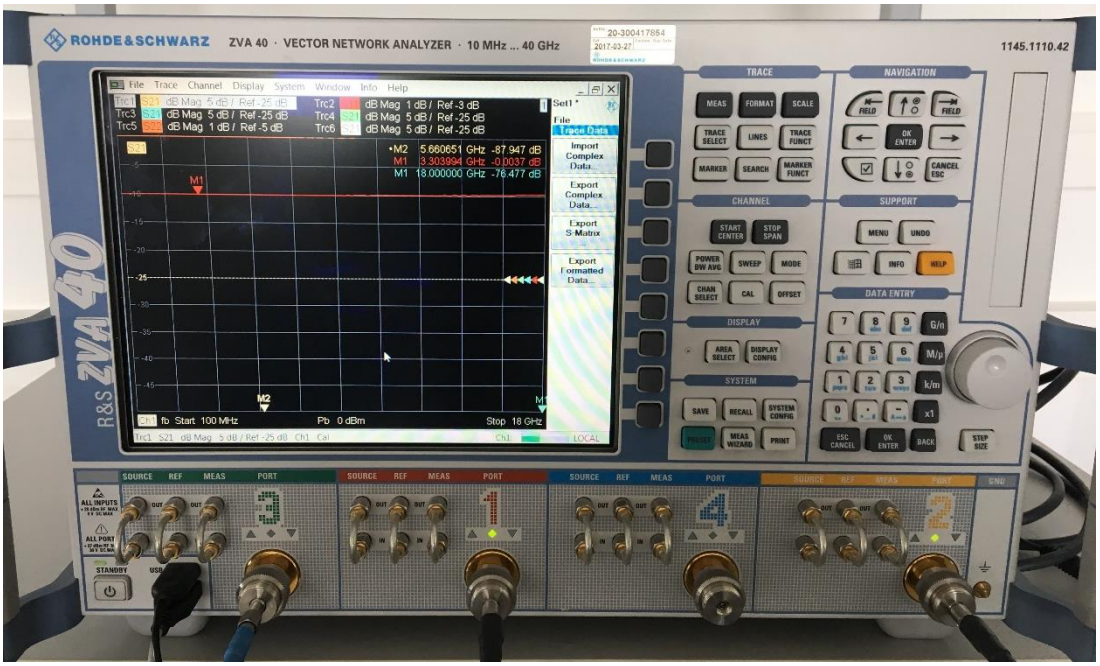


Figure 2.5 Rohde & Schwarz ZVA40 Vector Network Analyzer (VNA)

In Figure 2.6, three-port measurement is demonstrated. As shown in Figure 2.6, probe positions should be different directions (also similar for four-port measurements) because of the hardware issues of probe positioners that can be shown in Figure 2.6.

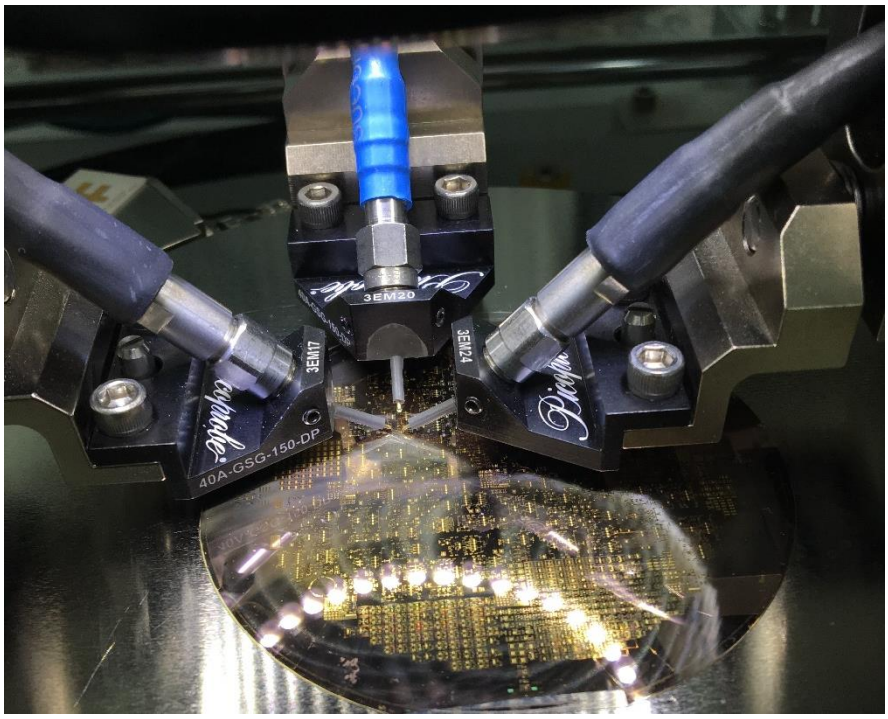


Figure 2.6 Probe positioners

3. DIVIDERS/COMBINERS

In this chapter, motivation, theoretical analysis, design considerations, simulation and measurement results of four divider/combiner structures which are four-way offset power combiner/divider, ring power divider/combiner with two-way, three-way phase shifted Wilkinson power divider/combiner and corporate power divider structures with four-way, are presented in detail.

3.1. Offset-Divider/Combiner

Top view of simple layout of the Offset-Divider/Combiner is shown at Figure 3.1. Left side of the layout has one input port. Right side has four output ports. In this work, 1:4 offset-divider is demonstrated.

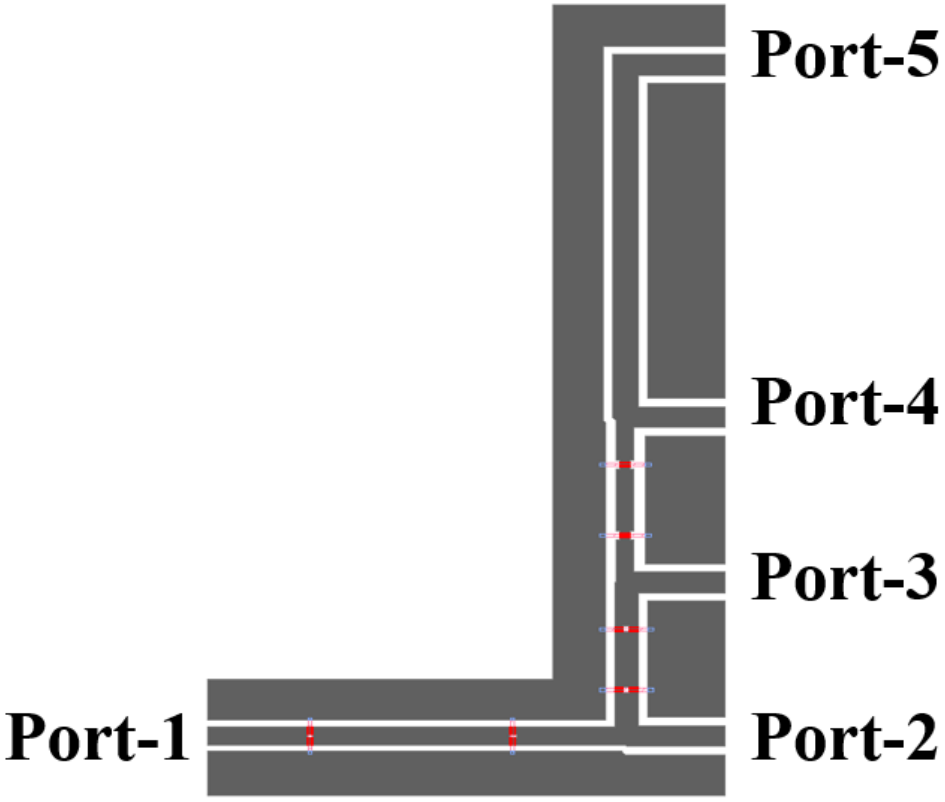


Figure 3.1 Simple Layout of the Offset Divider/Combiner

3.1.1. Analysis of Offset-Divider/Combiner

Offset-Divider in this thesis has 4 phase shifted output ports. Port numbers are given in Figure 3.1. Taking reflection from Port-2 as reference port (0°), reflections from Port-3, Port-4 and Port-5 will have 90°, 180° and 270° phase shifts respectively. Between neighboring output ports, there will be 90° phase difference. This phase shift provides phase delays for the reflection cancellation as given in Figure 3.2.

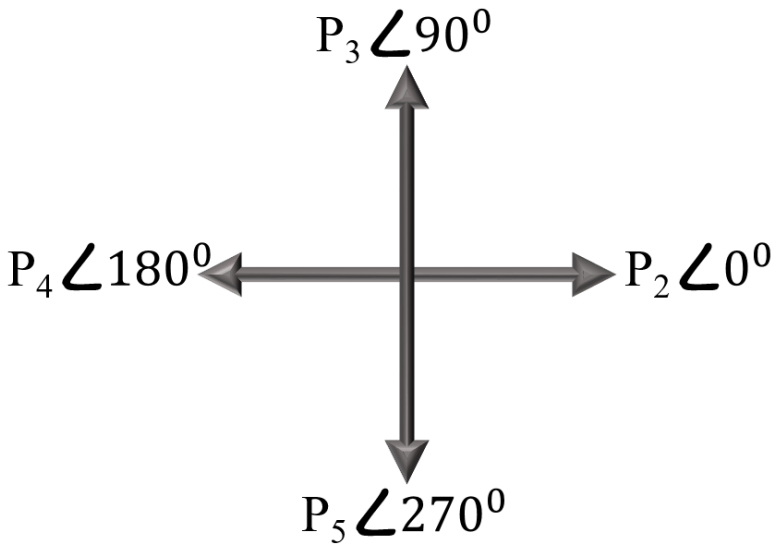


Figure 3.2 Vector diagram of relative phases of reflections from the output ports

Proposed circuit model of 1:4 offset-divider is demonstrated below in Figure 3.3. When performing calculations, input port and output ports impedances were assumed as arbitrary variables to obtain a generalized solution. Therefore, input and output ports were terminated as Z_{L1}, Z_{L2}, Z_{L3}, Z_{L4} and Z_{L5} as shown in Figure 3.3. Similarly, power division ratio of the offset divider was calculated as non-equivalent arbitrary split. In addition, all equations and calculations are performed for lossless circuit elements.

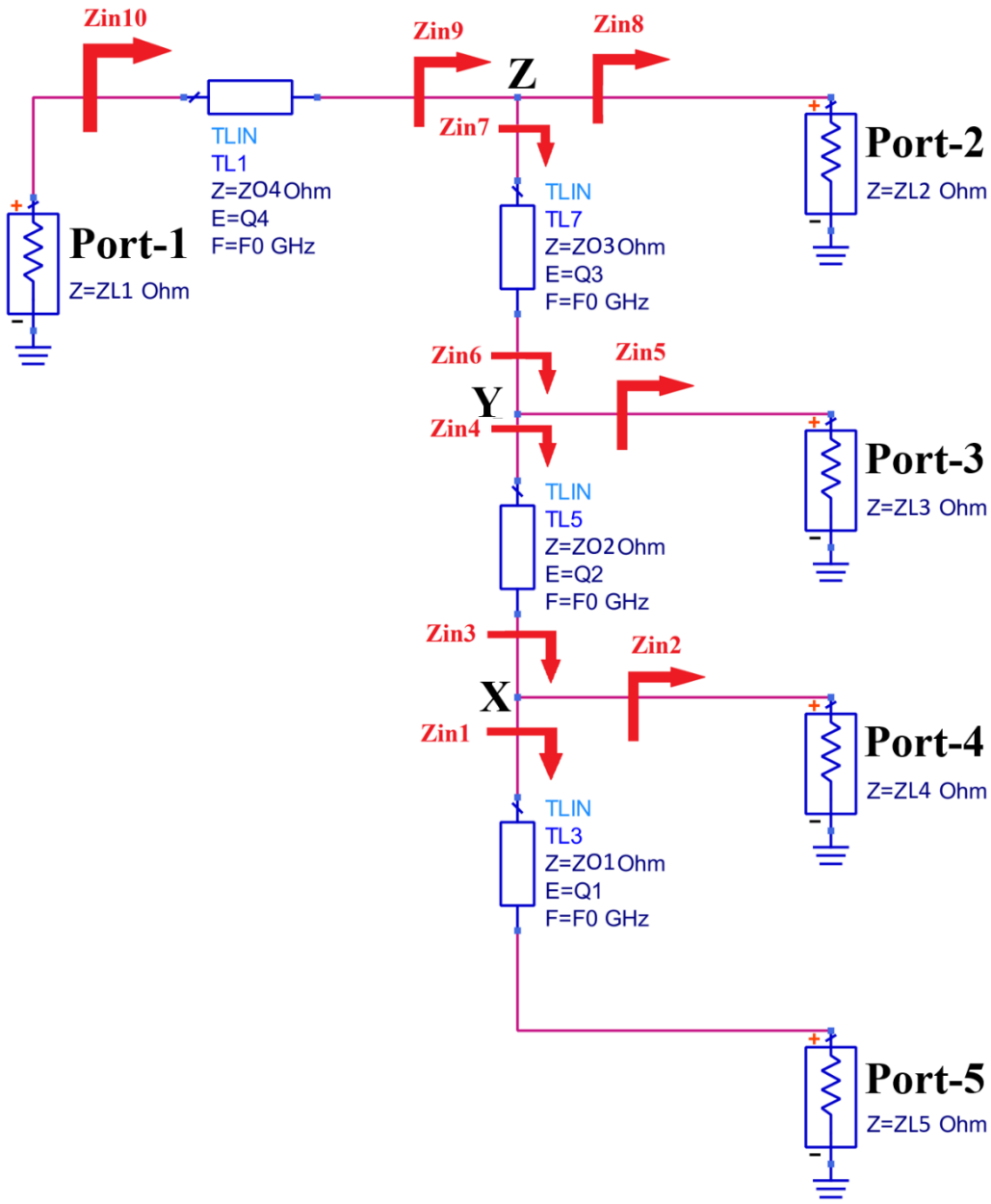


Figure 3.3 Schematic view of the 1:4 Offset-Divider

From the impedance equation of transmission line [17], input impedance can be calculated with equation below (3.1);

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan Q}{Z_0 + jZ_L \tan Q} \tag{3.1}$$

where Z_0, Z_{in}, Z_L represent the characteristic impedance of the transmission line, input impedance and load impedance, respectively. Q is the electrical length of the transmission

line that is βl (where β is propagation constant ($2\pi/\lambda$) and l is physical length of the transmission line).

All input impedances in this section are found by using equation (3.1). As indicated in Figure 3.3, Z_{in1} and Z_{in2} are calculated using equations (3.2) and (3.3) as

$$Z_{in1} = Z_{o1}\frac{Z_{L5} + jZ_{o1}\,tan\,Q_1}{Z_{o1} + jZ_{L5}\,tan\,Q_1} \tag{3.2}$$

$$Z_{in2} = Z_{L4} \tag{3.3}$$

where Q_1 and Z_{o1} represent electrical length and characteristic impedance of the TL3 respectively. Z_{L5} and Z_{L4} are term impedances of the Port-4 and Port-5 that are shown in Figure 3.3.

Power division ratio at node X that is shown in Figure 3.3 is calculated below equations (3.4) and (3.5).

$$P_5 = \frac{V_x^2}{Z_{in1}} \qquad P_4 = \frac{V_x^2}{Z_{in2}} \tag{3.4}$$

$$\frac{P_5}{P_4} = \frac{n}{m} \qquad \frac{Z_{in1}}{Z_{in2}} = \frac{m}{n} \tag{3.5}$$

where P_4 and P_5 are the power at Port-4 and Port-5 respectively, V_x is the voltage at node X, m and n represent the power coefficients at Port-4 and Port-5.

Input impedance by combining Port-4 and Port-5 is represented as Z_{in3} that is shown in Figure 3.3. It can be calculated from parallel combination of Z_{in1} and Z_{in2} impedances that is given in equation (3.6)

$$\begin{aligned} Z_{in3} = Z_{in1} \,//\, Z_{in2} &= \frac{Z_{in1}Z_{in2}}{Z_{in1} + Z_{in2}} \\ &= \frac{Z_{L4}Z_{o1}(Z_{L5} + jZ_{o1}\,tan\,Q_1)}{Z_{o1}(Z_{L5} + jZ_{o1}\,tan\,Q_1) + Z_{L4}(Z_{o1} + jZ_{L5}\,tan\,Q_1)} \end{aligned} \tag{3.6}$$

Substituting Eq. 3.5 into Eq. 3.6 yields equation (3.7)

$$Z_{in3} = \frac{Z_{in1}Z_{in2}}{Z_{in1} + Z_{in2}} = \frac{\frac{m}{n}Z_{in2}^2}{\frac{m+n}{n}\,Z_{in2}} = \frac{m}{m+n}Z_{in2} = \frac{m}{m+n}Z_{L4} \tag{3.7}$$

Similar approaches are followed for node *Y* and *Z* in order to find other input impedances at the offset divider (Figure 3.3).

Input impedance of the whole offset divider and input port impedance are represented as Z_{in10} and Z_{L1} that is shown in Figure 3.3. Calculation of these impedances are shown in equations below (3.8 and 3.9).

$$Z_{in10} = Z_{o4}\frac{Z_{in9} + jZ_{o4}\,tan\,Q_4}{Z_{o4} + jZ_{in9}\,tan\,Q_4} \tag{3.8}$$

$$Z_{L1} = Z_{in10}^{*} \tag{3.9}$$

where Z_{in10}^{*} is the complex conjugate of the input impedance of the whole offset power divider.

In the design section, in order to achieve 90° phase difference between output port reflections, lengths of the transmission lines are chosen as λ/8 at center frequency (f_c), that is 10 GHz. Reflection cancellation will be perfect for nf_c (n=1, 2, 3, 5, 6, ….). For frequencies below or above the center frequency, reflection cancellations will not be perfect; however, proportional to distance from the center frequency, there will still be a certain degree of reflection cancellation. In worst cases that are $4nf_c$ (n=0, 1, 2, 3…), reflections from output ports will be in the same directions/phases [18]. For these worst cases, offset divider acts as in-phase divider (e.g. Wilkinson power divider).

Termination impedances of the input port and output ports are designed as 50 Ω. In addition, power division ratio of offset divider is considered as equal split at the output ports. Therefore, power ratio should be 1:3 at node *Z*. With the same proportion, current ratio should be 1:3. Therefore, impedances of Z_{in7} and Z_{in8} can be shown as in the equations below (3.10 and 3.11).

$$Z_{in8} = 3Z_{in7} = 50\ \Omega \tag{3.10}$$

$$Z_{in7} \cong 16.67\ \Omega \tag{3.11}$$

Parallel combination of the Z_{in7} and Z_{in8} is equal to Z_{in9}. Using equation 3.6, Z_{in9} is calculated as

$$Z_{in9} = Z_{in7} // Z_{in8} = 25\ \Omega \tag{3.12}$$

Similar approaches are taken for node *X* and node *Y*. Power ratio should be 1:2 at node *Y* and 1:1 at node *X* for the offset divider in order to provide equal split at output ports. All input impedances can be found as indicated in Figure 3.4.

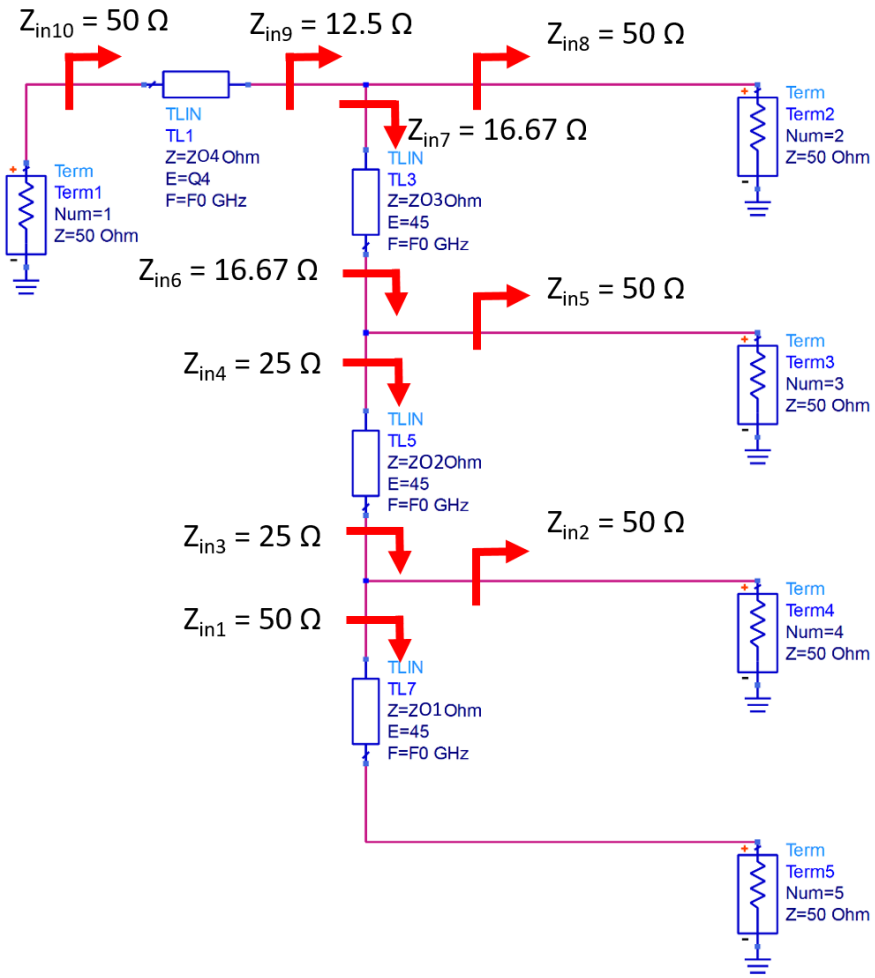
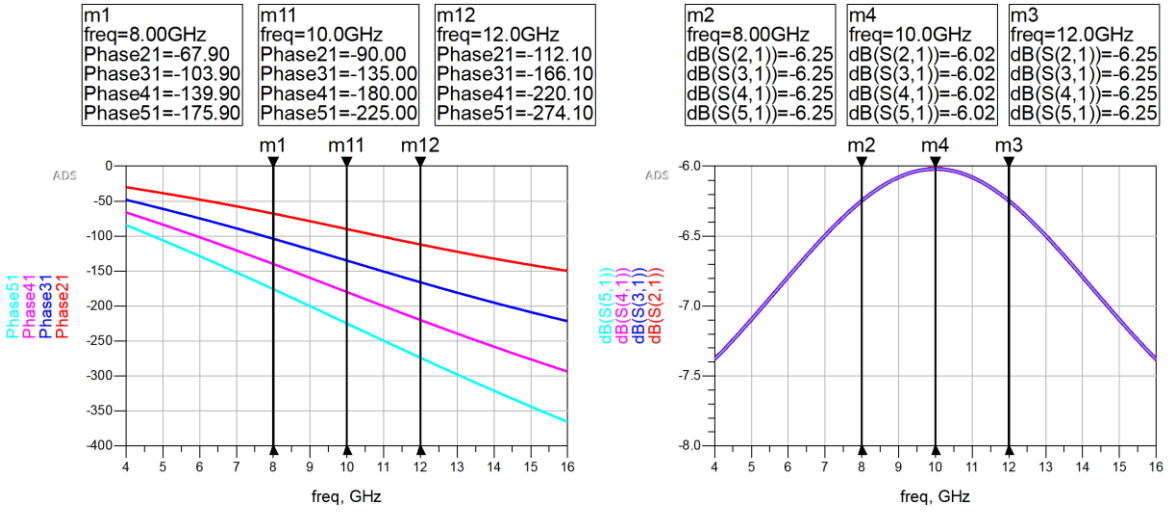


Figure 3.4 Schematic view of 1:4 Offset-Divider with calculated impedances

Characteristic impedances of the transmission lines are calculated using equation 3.1. Their electrical lengths are also determined. All impedances and electrical lengths of transmission lines are shown in Figure 3.4.

3.1.2. Design Process and Simulation Results of Offset-Divider/Combiner

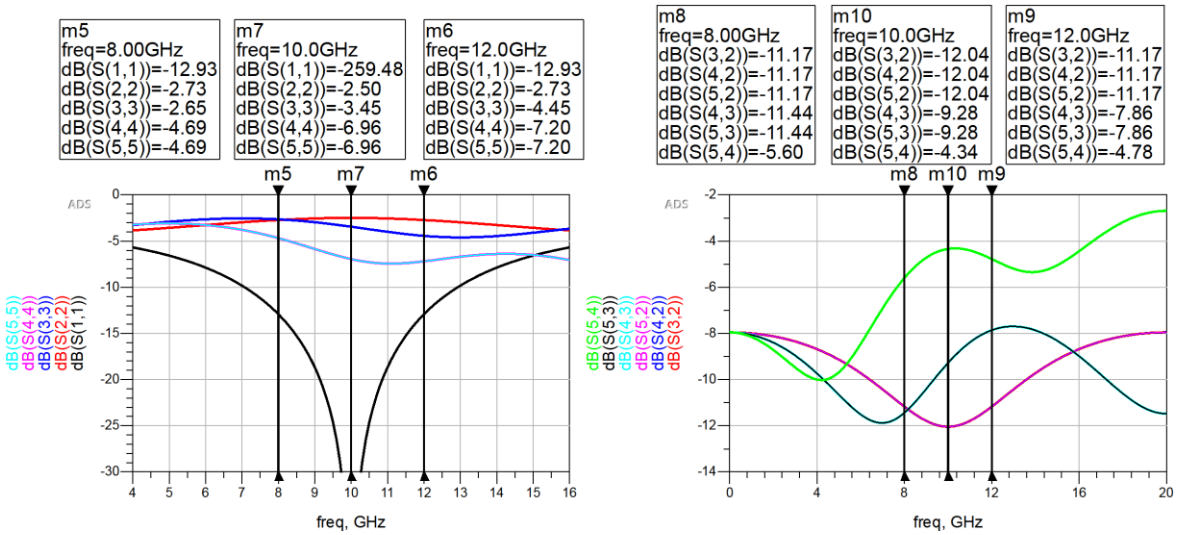
In this section, design techniques and 3D EM simulation results of the proposed offset divider are presented. Firstly, offset-divider/combiner is constructed with ideal (lossless) circuit elements using ADS simulation program. Port-1 is the input port, whereas Port-2 to Port-5 are the output ports of the designed offset-divider. Schematic view of the offset-divider/combiner with ideal circuit elements is shown in Figure 3.4. Simulation results of ideal offset-divider/combiner are demonstrated in figures below (Figure 3.5 and Figure 3.6).



(a) (b)

Figure 3.5 Simulation results of ideal offset-divider/combiner

a) Phase reflections b) insertion losses at Output ports



(a) (b)

Figure 3.6 Simulation results of the ideal offset-divider/combiner

a) reflection losses b) output ports isolations

1 to 4 offset divider with operation frequency bandwidth of 8-12 GHz is designed as an equal power splitter by using ADS simulation program. λ/8 length transmission lines were designed to create 90° phase difference between reflections from output ports and their characteristic impedances were chosen as specified in equations above. CoPlanar Waveguide (CPW) technology is used at layout implementation stage.

Three λ/8 length transmission lines and one λ/4 length transmission line are required in order to construct proposed offset divider. Total length of these transmission lines is approximately 7.7 mm considering the operation frequency band without using any miniaturization techniques. Therefore, one of the important aims in this work was to reduce the footprint of the divider. More than one miniaturization techniques which are the π-shaped structure methodology and meandering the transmission lines are utilized during the implementation of the transmission lines.

Miniaturization steps for one of the transmission lines in this offset divider, which has λ/4 length and has 25 Ω characteristic impedance, is given in Figure 3.7 below. Firstly, transmission line is constructed with ideal circuit components. Values of the ideal circuit elements are tuned in order to fit its simulation results with ideal transmission line results

especially at the operation frequency bandwidth. After determining the values of ideal circuit components, transmission line is realized according to the specified values. Schematic views of the 3 different circuits (a- ideal transmission line, b- miniaturized transmission line with ideal components, c- realized miniaturized transmission line via ADS layout) are shown in Figure 3.7 and layout of realized transmission line is shown in Figure 3.8. Comparisons of these 3 different transmission lines' results are given in Figure 3.9. Their reflection responses and phases are quite similar at operation frequency band.

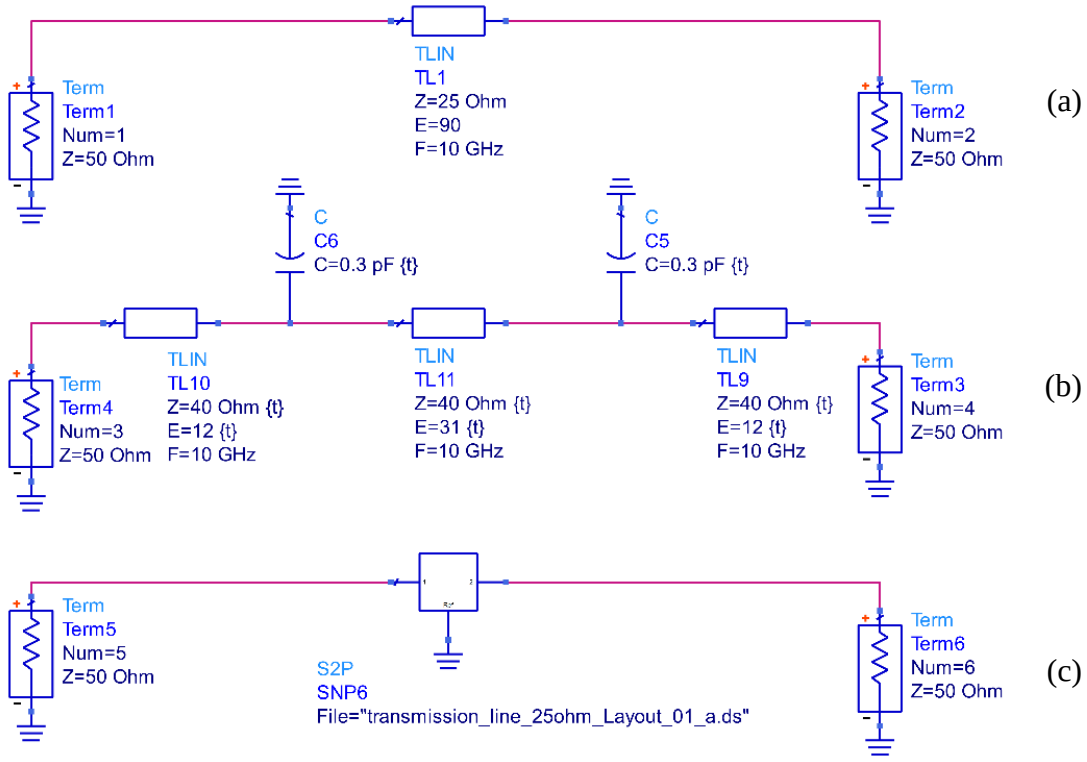


Figure 3.7 Schematic view of the (a) ideal transmission line, (b) miniaturized transmission line with ideal components and (c) realized miniaturized transmission line

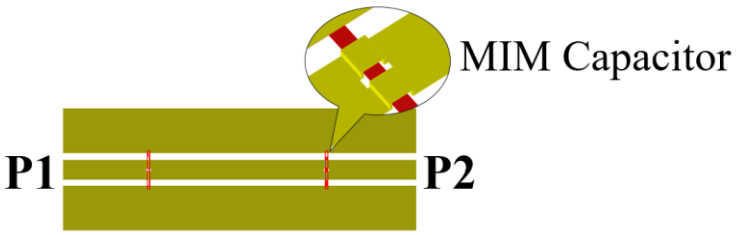
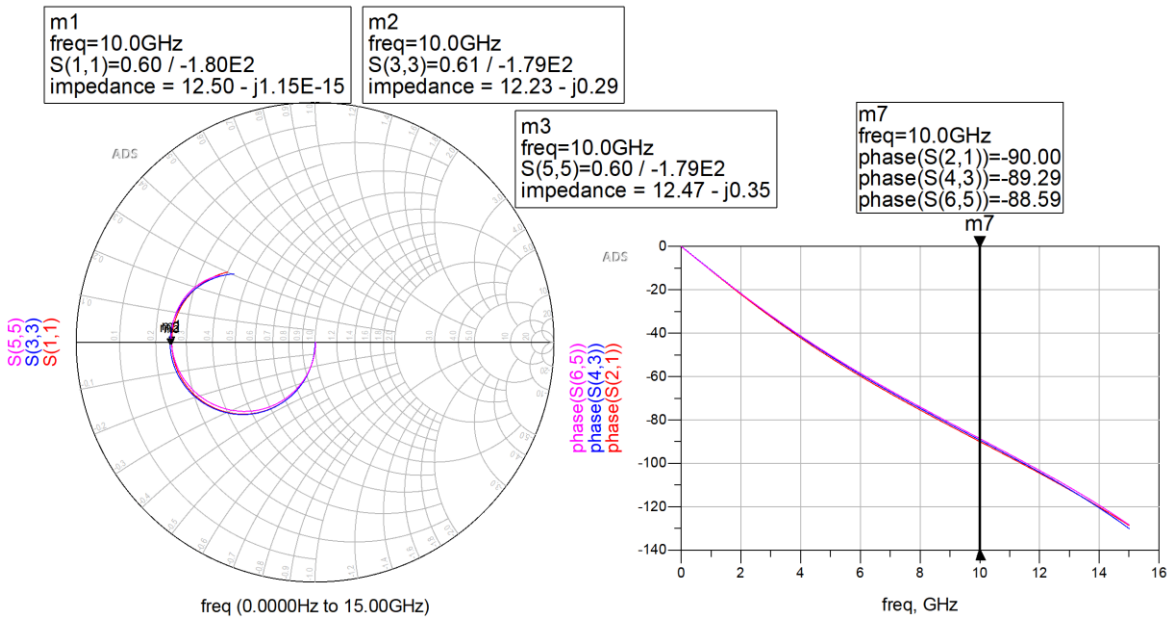


Figure 3.8 Layout view of miniaturized CPW transmission line



(a) (b)

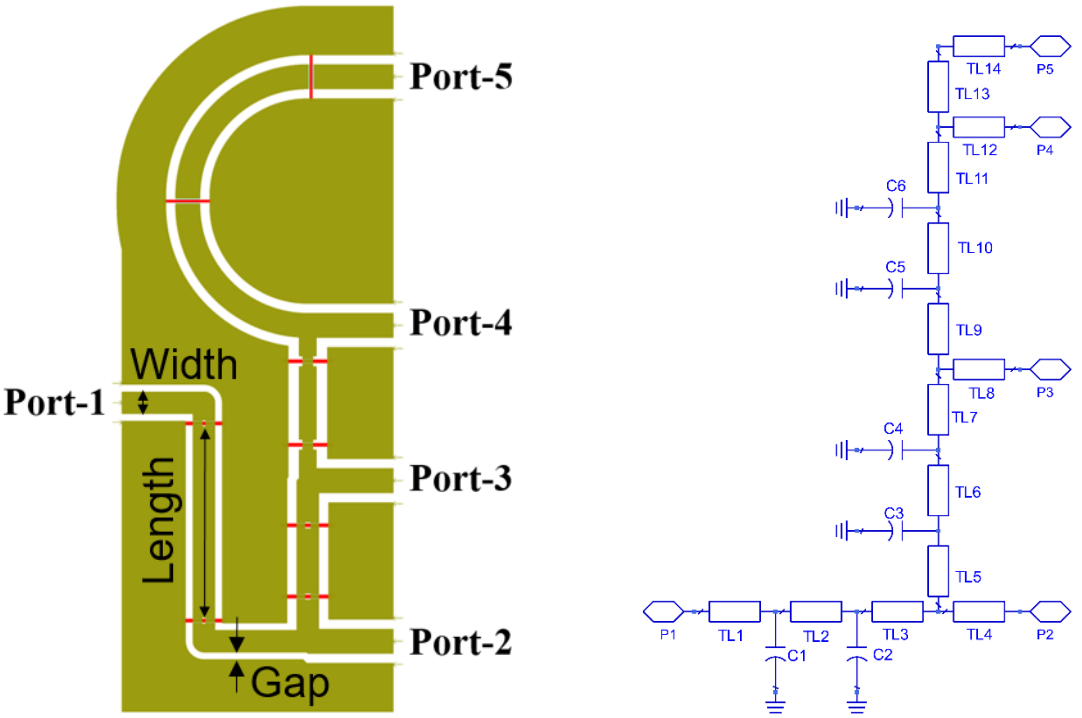
Figure 3.9 Comparison of the simulation results of transmission lines
a) Input reflection responses b) S21 phases

Rectangular footprint would be approximately 18mm^2 and effective footprint would be 5mm^2, if none of the miniaturization techniques were applied. By using miniaturization techniques, the footprint of the designed CPW offset divider reduced to 2.2mm^2. Both rectangular and effective footprint calculations lead to similar values for the area of this designed offset divider. Therefore, effective footprint of the offset divider is reduced approximately 55 percent and rectangular footprint is reduced approximately 90 percent. As a result, using miniaturization techniques in the design stage reduces the cost significantly.

After all transmission lines were miniaturized with the techniques described in section 2, final layout of the proposed 1:4 CPW offset divider is designed with the help of ADS simulation program. Dimensions of the components for the designed CPW offset divider are given in Table 3.1. Layout and schematic image of proposed offset divider are shown respectively in Figure 3.10.

Table 3.1 Dimensions of the components at the proposed CPW Offset Divider

Component Name	Width (µm)	Gap (µm)	Length (µm)	Component Name	Width (µm)	Gap (µm)	Length (µm)
TL1	90	30	412	**TL11**	70	45	75
TL2	90	30	798	**TL12**	100	40	265
TL3	90	30	412	**TL13**	100	40	1515
TL4	100	40	265	**TL14**	100	40	265
TL5	90	40	124	**C1**	90	30	14
TL6	90	40	280	**C2**	90	30	14
TL7	90	40	124	**C3**	85	42	13
TL8	100	40	265	**C4**	85	42	13
TL9	70	45	75	**C5**	54	53	13
TL10	70	45	330	**C6**	54	53	13



(a) (b)

Figure 3.10 (a) Layout and (b) Schematic view of the proposed CPW offset divider

3D EM simulation results of the proposed 1:4 offset divider are given in Figure 3.11. As shown in Figure 3.11.a, insertion losses of the output branches are better than 1dB at the center frequency (10 GHz). Phase differences of the output ports are approximately 45˚±2˚ at the center frequency. Therefore, phase shifts of reflections at the output ports are 90˚±5˚. Isolations of the output ports are lower than 9 dB, except isolation between Port-4 and Port-

5. Input return loss is lower than 12 dB in the operation frequency band that is from 8 GHz to 12 GHz.

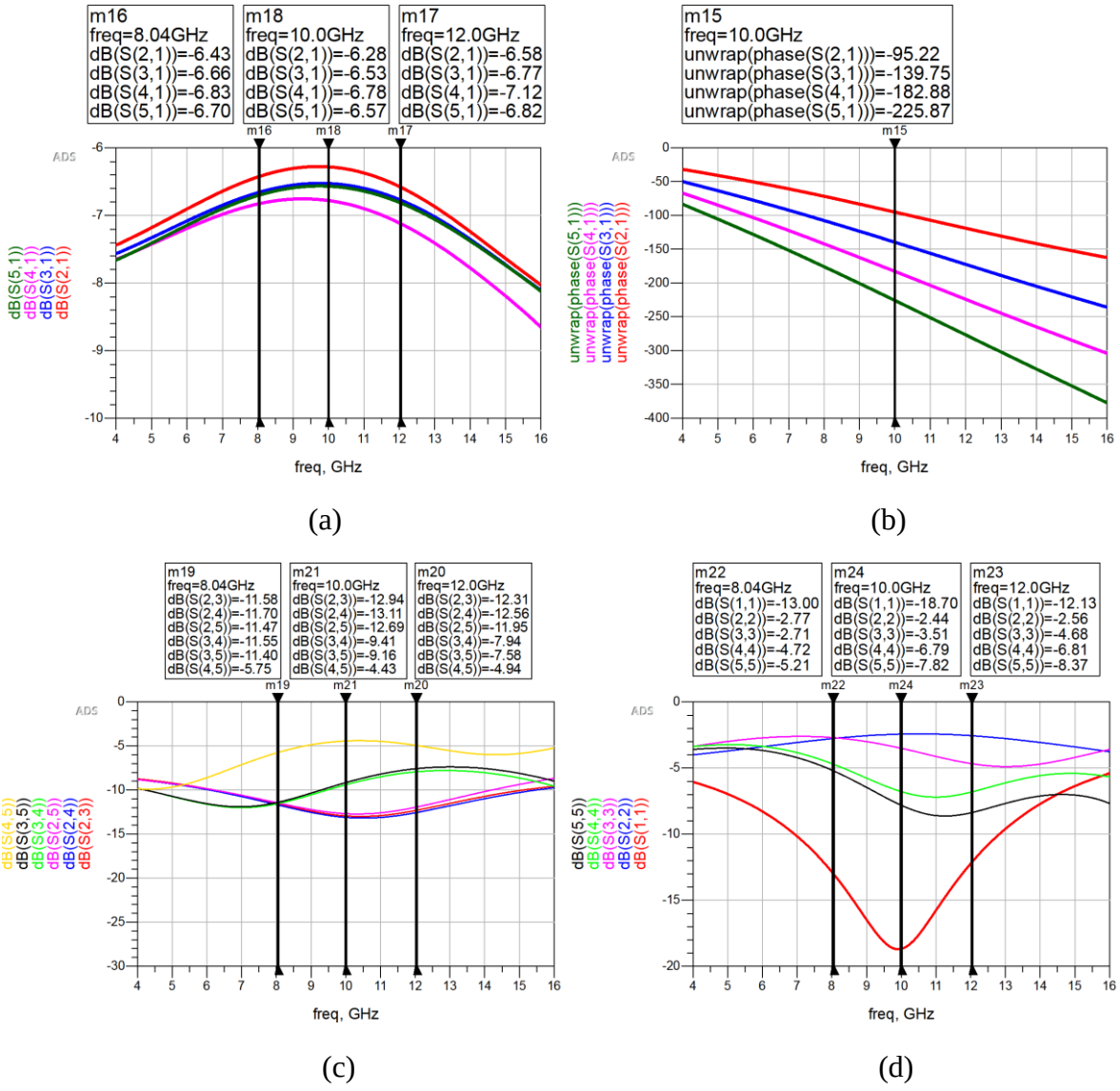
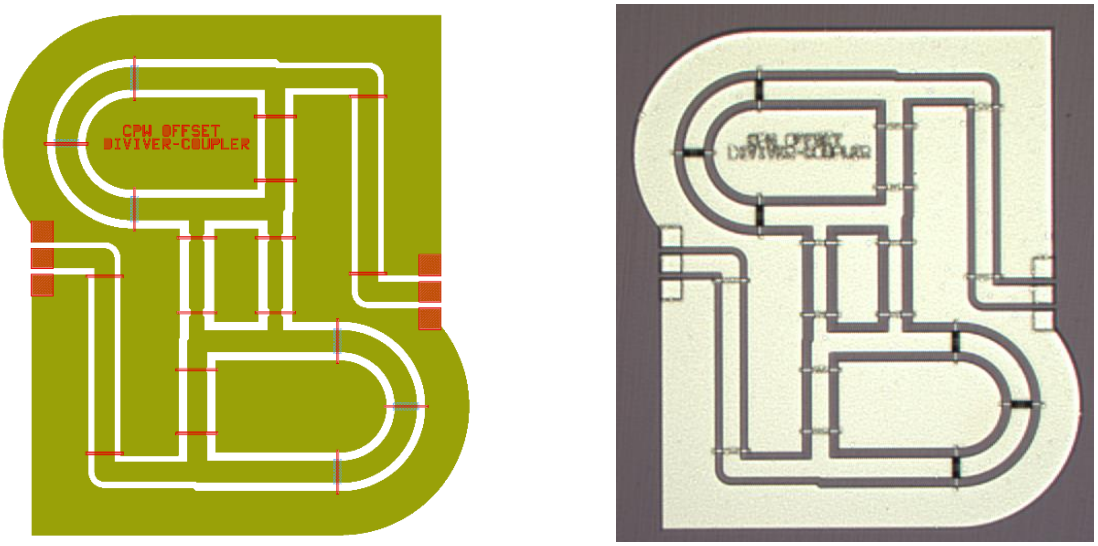


Figure 3.11 Simulation results of the designed CPW offset divider a) Insertion losses b) Phases c) Isolations of output ports d) Input and output return losses

3.1.3. S-Parameter Measurements and Comparison of the Measurements with Simulation Results

In this section, S-parameter measurements of the designed 1:4 offset divider results and comparison of the measurement results with simulation results are presented. Since the proposed offset divider has 5 ports (1 input and 4 output ports), constructed structures are connected back to back in order to evaluate performance of fabricated structures with 2 port

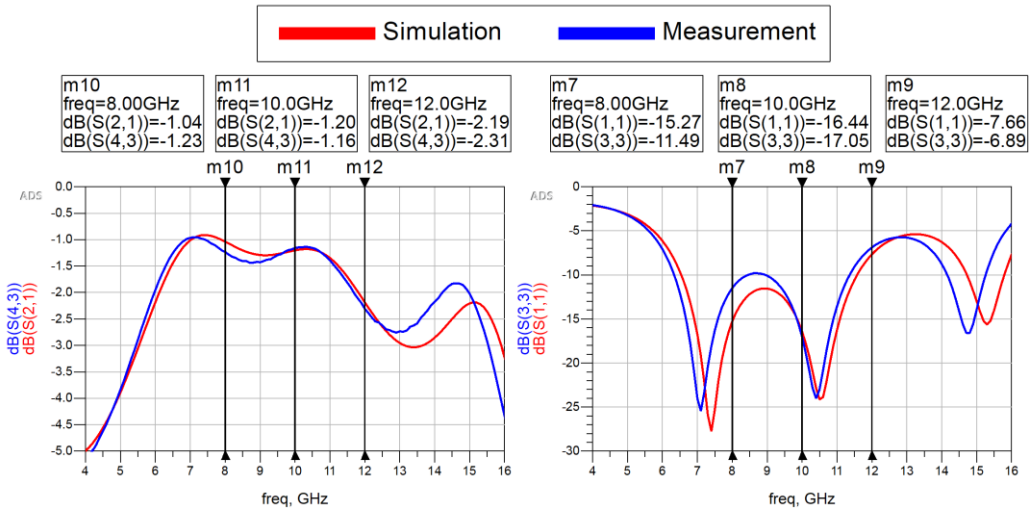
measurements. Photomask view and microscope image of fabricated back-to-back CPW offset-dividers are shown in Figure 3.12, respectively.



(a) (b)

Figure 3.12 (a) Masked view, (b) Microscope image of the back to back offset divider

EM simulation result of the finalized layout and measurement result of the fabricated CPW offset divider are shown in Figure 3.13. Insertion losses and return losses are quite similar at the frequency band of interest.



(a) (b)

Figure 3.13 Comparison of the measurement and simulation results of the CPW offset divider a) Insertion losses b) Return losses

3.2. Ring Power Divider/Combiner

Wilkinson power divider is one of the well-known and commonly utilized power dividers due to its high isolation and low insertion loss. However, the simple WPD provides narrow-band isolation compared to the ring power divider/combiner structures [11]. When combining active circuit elements such as transistors or whole MMICs, port isolations at the frequencies in band and out of band play a crucial role in order to get rid of the unwanted feedback loops and oscillations [12]. In high power microwave circuits therefore, power dividers/combiners that have wide-band port isolations are preferred to minimize the risk of undesirable oscillations. In Figure 3.14, Simplified layout of the Ring Power Divider/Combiner is given.

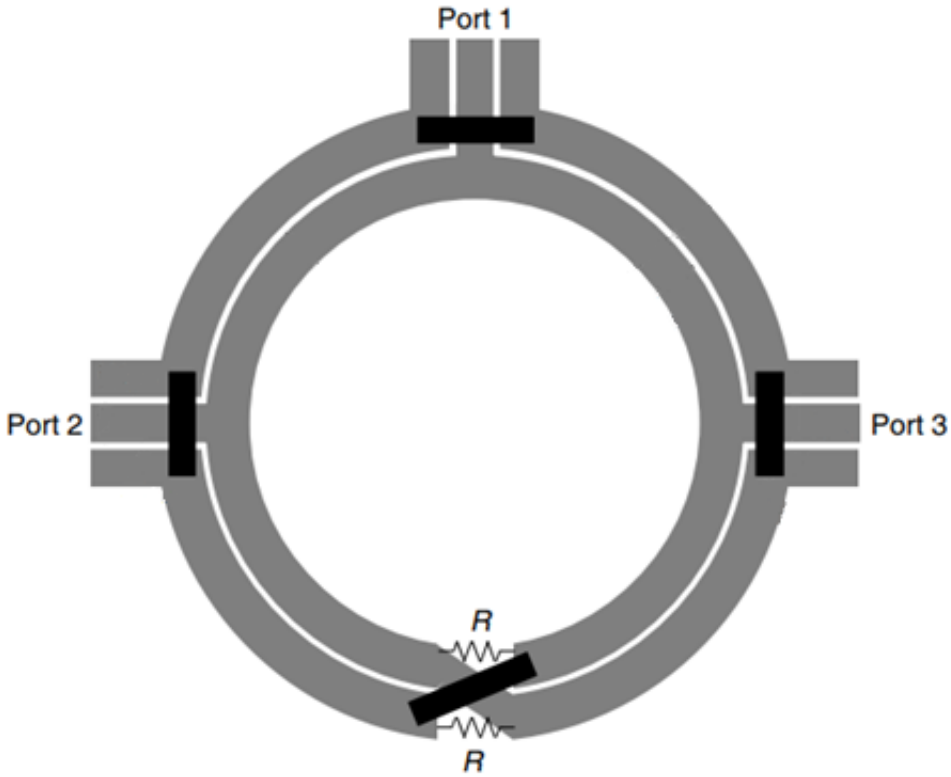


Figure 3.14 Simplified layout of the Ring Power Divider/Combiner

3.2.1. Analysis of Ring Power Divider

In this section, even and odd mode analysis of symmetrical ring power divider/combiner is represented. Simulation results of the ring power divider/combiner that is designed with ideal circuit elements are given.

In order to enhance isolation performance at the output ports (Port-2 and Port-3), crossover phase inverter structure shown in Figure 3.14 is implemented. As mentioned above, high and wideband isolation between output ports is significant for the prevention of unwanted amplifier feedback loop and oscillations. Instead of using resistors to isolate output ports, as is the case in Wilkinson power divider topology; 2 quarter-wavelength transmission lines, crossover phase inverter with two resistors between output ports are used to provide wideband isolation at output ports in the ring power divider/combiner (Figure 3.14). By using a crossover phase inverter, frequency independent 180^0 phase inversion is applied. Also, two quarter-wavelength transmission lines present very high (virtually open circuit) impedance at the output ports, when looked from the other output ports. Impedance matching at the output ports of the ring power divider/combiner is improved by using two resistors between these $\lambda/4$ transmission lines. Therefore, high and broadband isolation at output ports is ensured. Simple layout view of the ring power divider is seen in Figure 3.15.

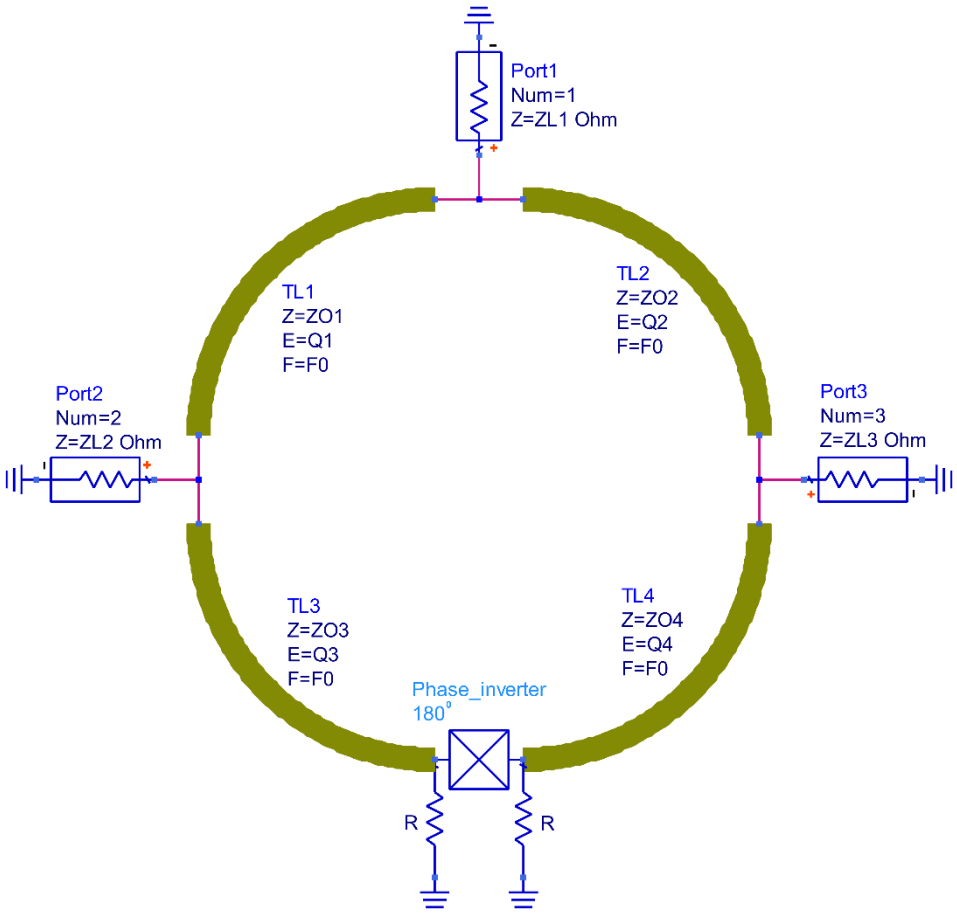


Figure 3.15 Simple layout view of the ring power divider

As given in Figure 3.15, Port1 is input port, Port2 and Port3 are output ports of designed ring power divider. When signal is coming from the input port (Port1), it propagates only through the Port2 and Port3. Equivalent circuit model for this case (Case #1) is given in Figure 3.16.

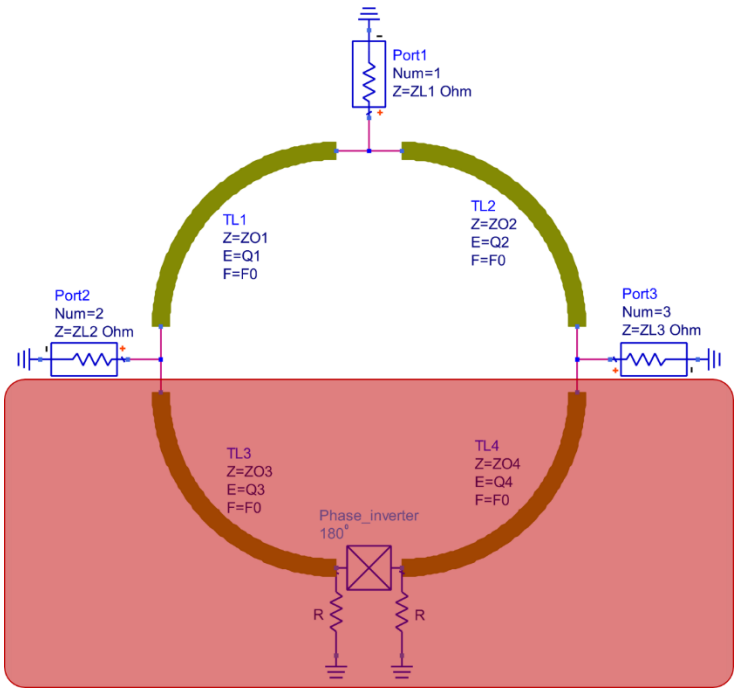


Figure 3.16 Circuit model of the ring power divider for the case#1

There will be no current flow through the shaded region, due to the high isolations between Port-2 and Port-3 that is shown in Figure 3.16. Therefore, input impedances of Port-1, which is denoted as Z_{L1}, can be written as shown in equation (3.13).

$$Z_{L1} = \frac{Z_{o1}^2}{Z_{L2}} \,//\, \frac{Z_{o2}^2}{Z_{L3}} = \left(\frac{Z_{L2}}{Z_{o1}^2} + \frac{Z_{L3}}{Z_{o2}^2}\right)^{-1} \tag{3.13}$$

where Z_{L2} and Z_{L3} are the input impedances of Port-2 and Port-3 respectively, Z_{o1} is characteristic impedance of the transmission line between Port-2 and input port, Z_{o2} is characteristic impedance of the transmission line between Port-3 and input port and all the transmission lines have $\lambda/2$ length at center frequency (f_0) of 10GHz.

In the unequal power division case, power is divided between Port-3 and Port-2 proportional to their input impedances. Therefore, ratio of the input impedances between the output ports gives the power ratio constant (k), which is calculated as in equation (3.14).

$$k = \frac{\frac{Z_{o1}^2}{Z_{L2}}}{\frac{Z_{o2}^2}{Z_{L3}}} = \frac{Z_{o1}^2 Z_{L3}}{Z_{o2}^2 Z_{L2}} \tag{3.14}$$

When the signal is injected at Port-2, it flows through the two paths. One of them flows to Port-1 and the other one is absorbed at the resistor. Circuit model of the power divider in this case (Case #2) is given in Figure 3.17. There will be no current flow at shaded region due to the even mode analysis.

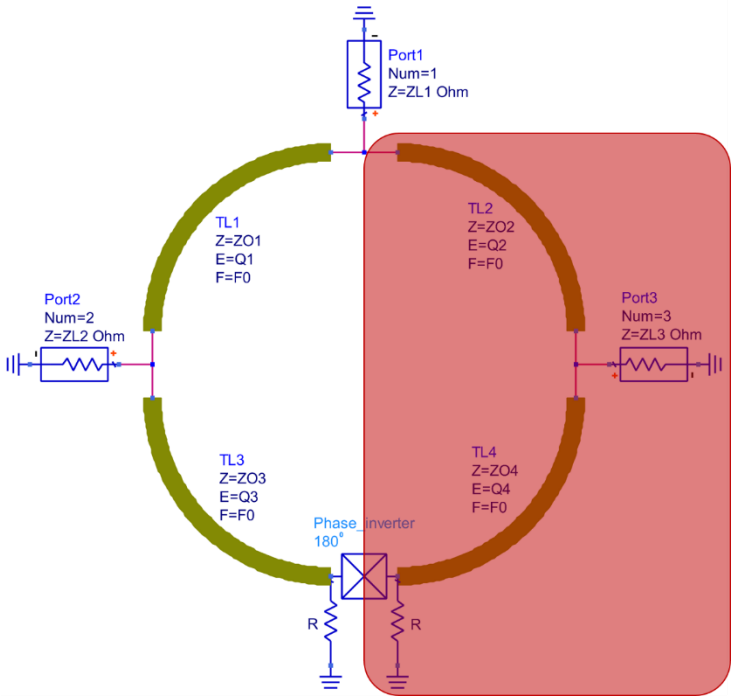


Figure 3.17 Circuit model of simple ring power divider for case#2

By performing impedance analysis of the circuit that is given at Figure 3.17, input impedance of Port-2 (Z_2) is calculated as in equation (3.15).

$$Z_{L2} = \frac{Z_{o1}^2}{Z_{L1}} \,//\, \frac{Z_{o3}^2}{R/2} = \left(\frac{Z_{L1}}{Z_{o1}^2} + \frac{R}{2Z_{o3}^2}\right)^{-1} \tag{3.15}$$

where Z_{o3} is characteristic impedance of the transmission line between 180° phase inverter and Port-2, R is the resistor at 180° phase inverter and all transmission lines have $\lambda/2$ length at center frequency (f_0) of 10 GHz.

When the signal is injected at Port-3, it passes through the same path with the above case. Therefore, input impedance of Port-3 is found as shown in equation (3.16).

$$Z_{L3} = \frac{Z_{o2}^2}{Z_{L1}} \,//\, \frac{Z_{o4}^2}{R/2} = \left(\frac{Z_{L1}}{Z_{o2}^2} + \frac{R}{2Z_{o4}^2}\right)^{-1} \tag{3.16}$$

where Z_{o4} is characteristic impedance of the transmission line between 180° phase inverter and Port-2.

By solving equations (3.13) and (3.14), characteristic impedances of the transmission lines (Z_{o1} and Z_{o2}) are found as in equations (3.17) and (3.18).

$$Z_{o1} = \sqrt{(1+k)Z_{L1}Z_{L2}} \tag{3.17}$$

$$Z_{o2} = \sqrt{\left(1 + {}^{1}/_{k}\right)Z_{L1}Z_{L3}} \tag{3.18}$$

By solving equations (3.15) and (3.17), characteristic impedance of the transmission line (Z_{o3}) is obtained as given in equation (3.19). By substituting eq. (3.18) into eq. (3.16), characteristic impedance of the transmission line (Z_{o4}) is found as in equation (3.20).

$$Z_{o3} = \sqrt{\left(1 + {}^{1}/_{k}\right)Z_{L2}\,{}^{R}/_{2}} \tag{3.19}$$

$$Z_{o4} = \sqrt{(1+k)Z_{L3}\,{}^{R}/_{2}} \tag{3.20}$$

In addition to these four equations above ((3.21), (3.22), (3.23) and (3.24)), injected signal from Port-1 flows through the branches. One of them flows from *TL*1 to *TL*3 direction, the other one flows from *TL*2 to *TL*4 direction that is shown in Figure 3.15. Because of the perfect isolation between output ports, signals passing through the branches should be equal in amplitude. Therefore, characteristic impedances of *TL*1 and *TL*3, *TL*2 and *TL*4 should be of the same magnitude as given in equations (3.21) and (3.22) below.

$$Z_{o1} = Z_{o3} \tag{3.21}$$

$$Z_{o2} = Z_{o4} \tag{3.22}$$

From Equations 3.5-3.10, values of Z_{o1}, Z_{o2}, Z_{o3}, Z_{o4} and R can be outlined as presented below in equations (3.23), (3.24) and (3.25).

$$Z_{o1} = Z_{o3} = \sqrt{(1+k)Z_{L1}Z_{L2}} \tag{3.23}$$

$$Z_{o2} = Z_{o4} = \sqrt{\left(1 + {}^{1}/_{k}\right)Z_{L1}Z_{L3}} \tag{3.24}$$

$$R = 2Z_{o1} \tag{3.25}$$

In the design calculations, input impedances of all three ports are taken as 50 Ω. Therefore, $Z_{L1} = Z_{L2} = Z_{L3} = 50\ \Omega$. Also, ratio of the power at output branches in ring power divider is considered as equal split (k=1). Therefore, shunt resistors and characteristic impedances of the transmission lines are found as shown in equations (3.26), (3.27) and (3.28) below.

$$Z_{o1} = Z_{o3} \cong 70.7\ \Omega \tag{3.26}$$

$$Z_{o2} = Z_{o4} \cong 70.7\ \Omega \tag{3.27}$$

$$R = 100\ \Omega \tag{3.28}$$

3.2.2. Design Process and Simulation Results of Offset-Divider/Combiner

In this section, design techniques and 3D EM simulation results of the designed ring power divider were presented. First of all, two-way ring power divider is constructed with ideal

lumped components by using calculated above values. Schematic view of the ring power divider was demonstrated in Figure 3.18.

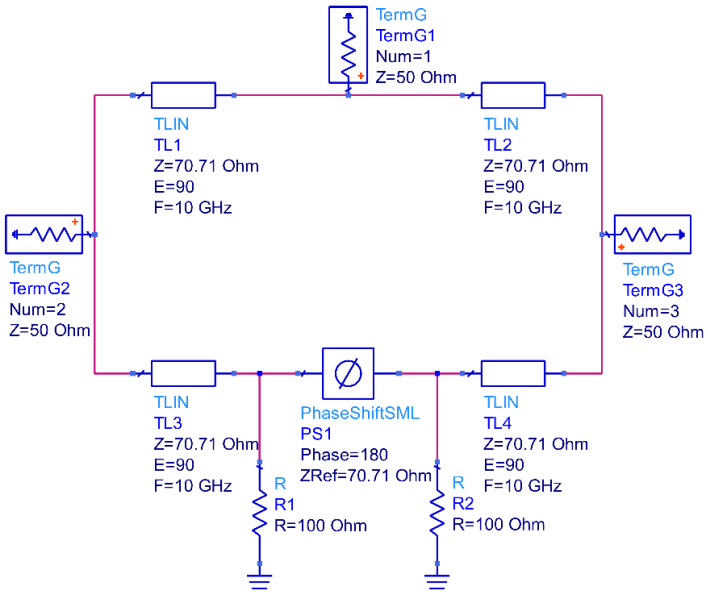
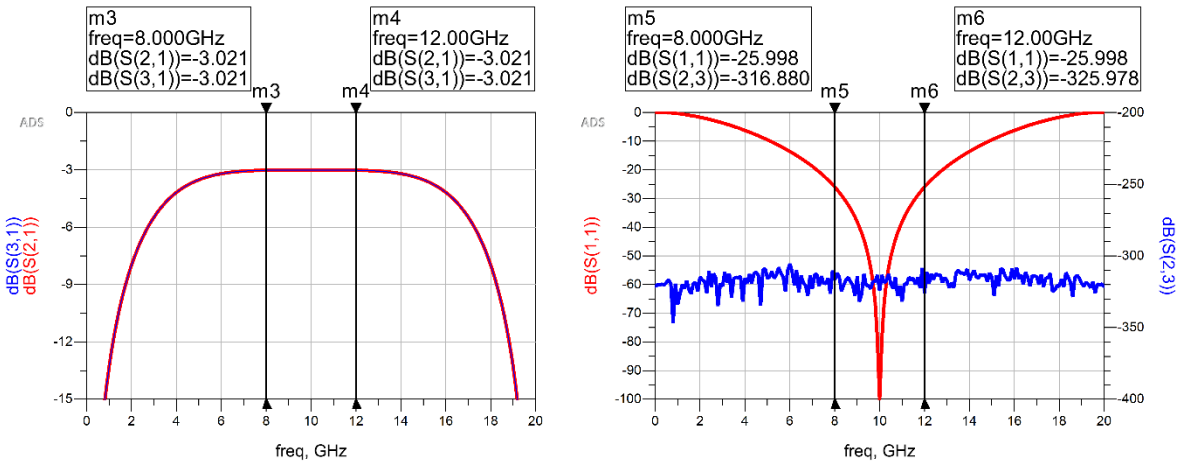


Figure 3.18 Simple Schematic view of the ring power divider with ideal circuit elements

Simulation results at the 0-20 GHz frequency band for the ring power divider with ideal circuit elements are seen in Figure 3.19. Insertion losses, input and output port reflections and isolation at the output ports are given in figures below.



(a) (b)

Figure 3.19 Simulation results of the ideal ring power divider a) insertion losses b) reflection at all ports (red line) and isolation at Output ports (blue line)

As also mentioned in Section 3.2.1, simple ring divider consists of four λ/4 length transmission lines. Therefore, standard ring power dividers occupy a forbiddingly large chip area in monolithic fabrication processes, rendering them impractical and too expensive to use in designs. Although ring power divider has great isolation at output ports, RF circuit designers do not prefer this type of power divider and combiner for the GaN based integrated circuits due to this space concern. Therefore, in this thesis work, ring power divider is improved by using miniaturization techniques. π-shaped structure methodology and meandering of the transmission lines are applied to miniaturize the circuit. As given in Figure 3.20, standard λ/4 transmission line and miniaturized λ/4 transmission line with 70.7 Ω characteristic impedances are compared in their dimensions. Transmission line length is reduced by approximately 30 percent.

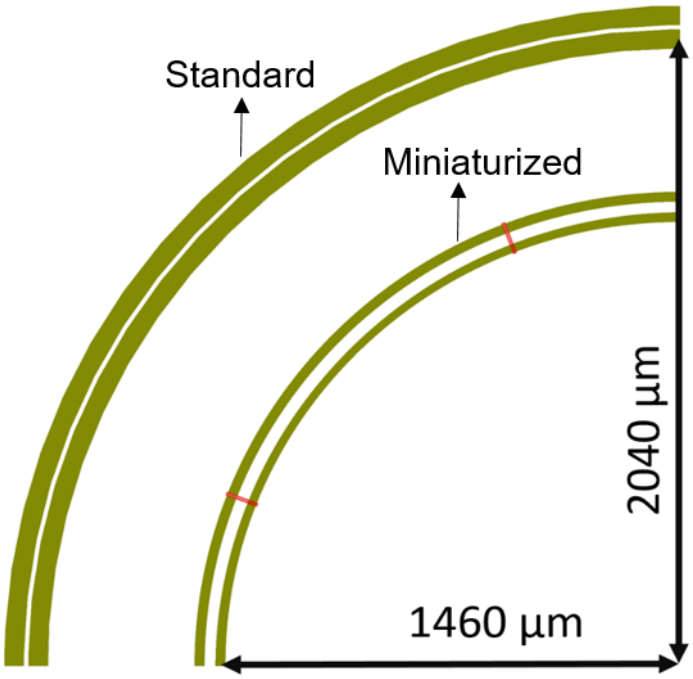
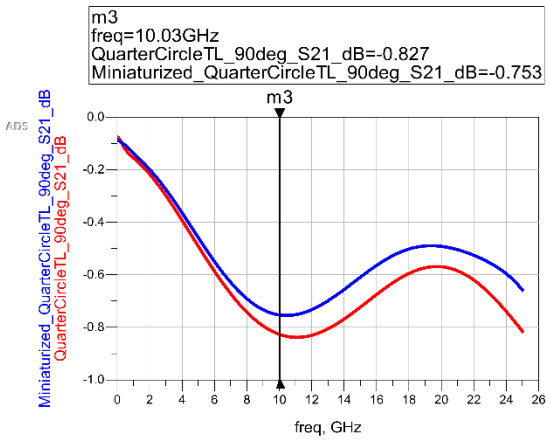
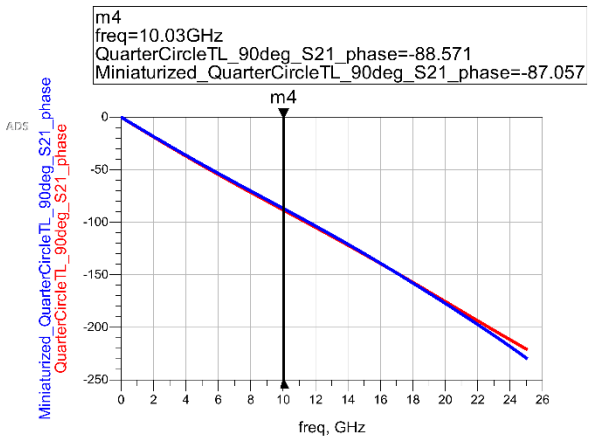


Figure 3.20 Layout view of standard transmission line and miniaturized transmission line

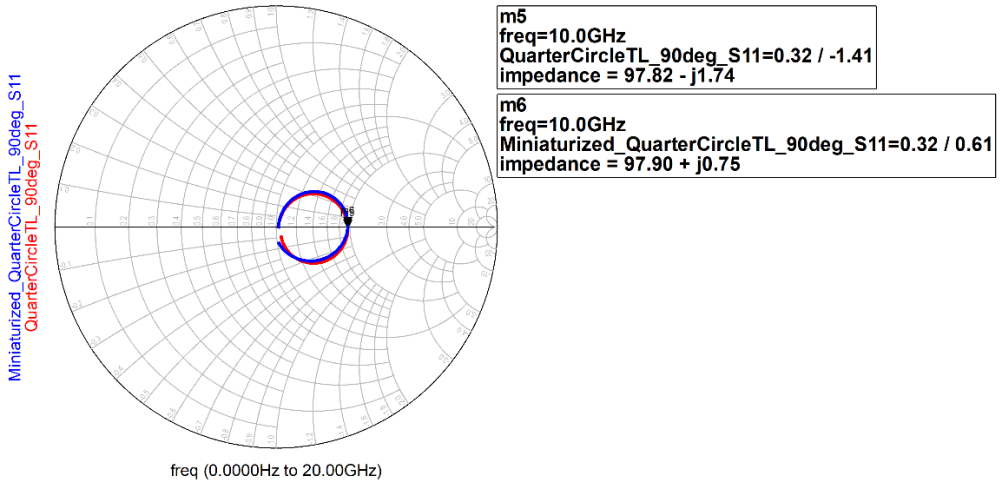
EM simulation results of these transmission lines are given in Figure 3.21. Red lines in these figures represent the result of the standard transmission line whereas the blue ones represent the miniaturized transmission line. Insertion losses, phases and reflection coefficients of the miniaturized transmission line are almost identical with the results of the standard transmission line.



(a)



(b)



(c)

Figure 3.21 Simulation results of the standard (red line) and miniaturized (blue line) transmission lines a) Insertion losses b) Phases c) reflection coefficients

Similar miniaturization techniques are also applied on transmission lines between output ports of the designed ring power divider. In addition, in order to take advantage of the otherwise wasted empty space inside the ring power divider, transmission lines between output ports are meandered inward towards the middle region of the ring power divider. Final layout design of the ring power divider is given in Figure 3.22. Layout of a standard (commercial) ring power divider is also given in Figure 3.22 for comparison purposes.

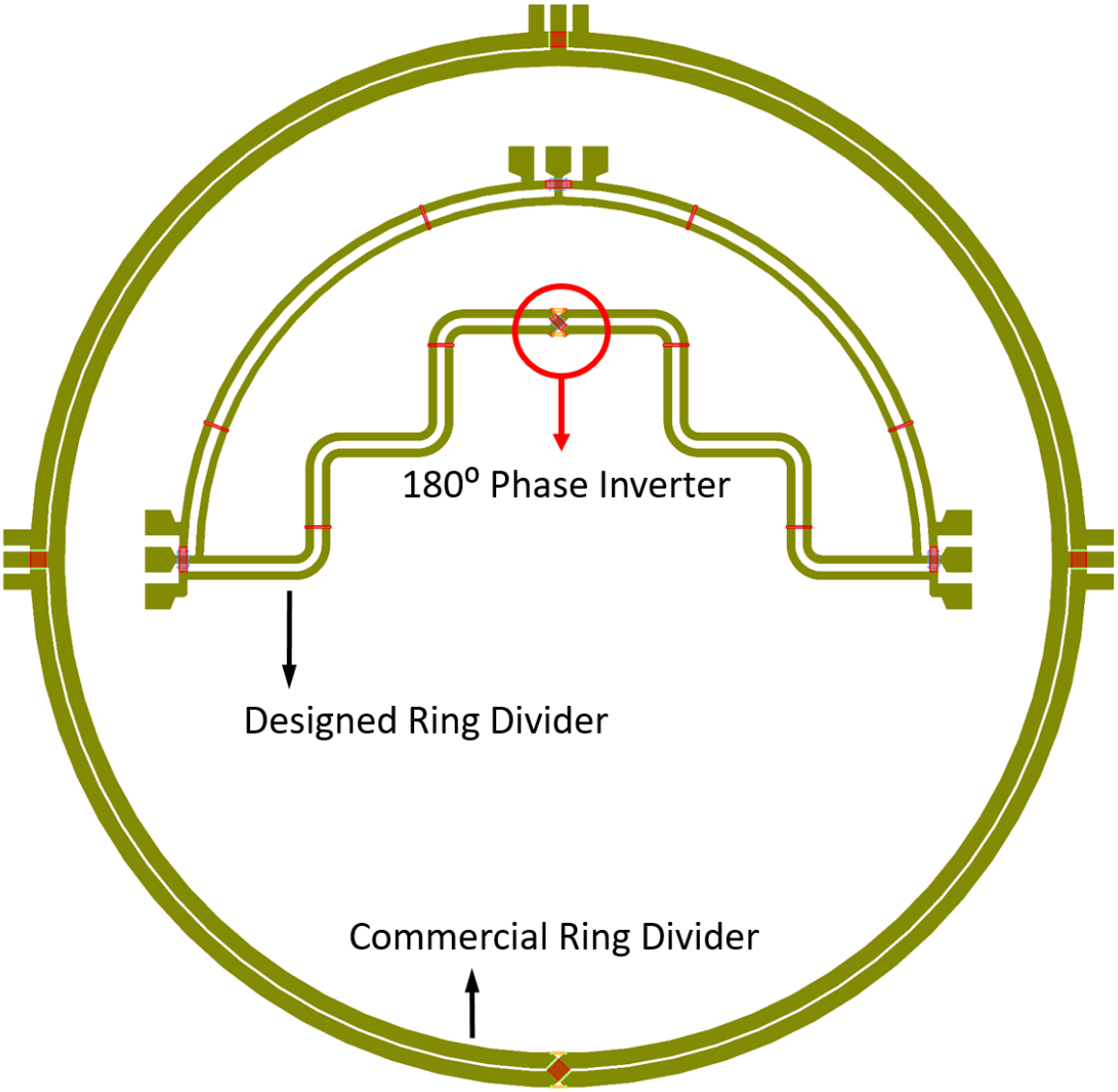


Figure 3.22 Layout view of the designed ring power divider (3.35 mm x 1.88 mm) and commercial ring power divider (4.50 mm x 4.45 mm)

Standard simple ring power divider at 10GHz center frequency occupy approximately 20 mm^2 rectangular footprint and 15.6 mm^2 effective footprint since it consists of four λ/4 transmission lines without using any miniaturization techniques. In other words, effective area of the designed standard ring power dividers in [19]-[22] are approximately equal to the expression in equation 3.29.

$$Area = \pi\left(\frac{\lambda}{2\pi}\right)^2 = \frac{\lambda^2}{4\pi} \tag{3.29}$$

By using the miniaturization techniques explained in this thesis work, rectangular footprint of the designed ring divider shrank to 6 mm^2 and effective footprint is determined as 4.4 mm^2. Therefore, rectangular footprint of the ring power divider is reduced by approximately 70 percent and effective footprint was reduced by approximately 72 percent. Consequently, designed ring divider has become less expensive to fabricate in GaN processes, thus more suitable for high power microwave integrated circuit applications.

In this design, frequency independent 180° phase inverter was used in order to provide high isolation at wide band. Air-bridge structure is used at the metal-metal crossover in the phase inverter section, as shown in Figure 3.23. SEM image of the metal-metal crossover in the phase inverter section is given in Figure 3.24. Height of the air-bridge at phase inverter is critical for this design because of the extra parasitic effects and undesirable mode excitation. Therefore, at the final design stage, gap and width of the transmission lines are fine-tuned depending on the results of the ADS Momentum simulator.

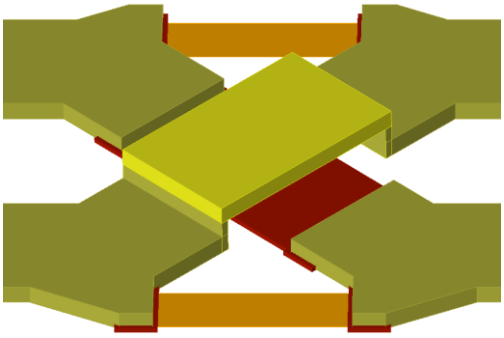


Figure 3.23 Layout view of the 180° phase inverter

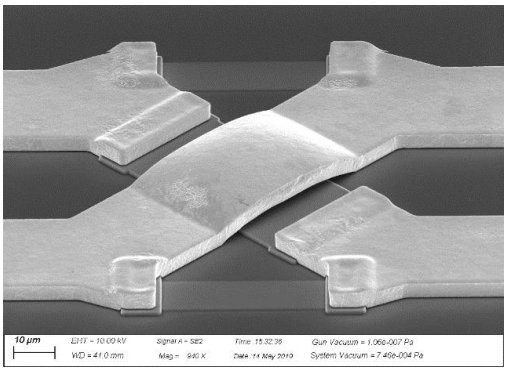


Figure 3.24 SEM image of the 180° phase inverter

Layout image of proposed ring power divider with component names is given in Figure 3.25. Layout dimensions of the components for the designed ring power divider are seen in Table 3.2.

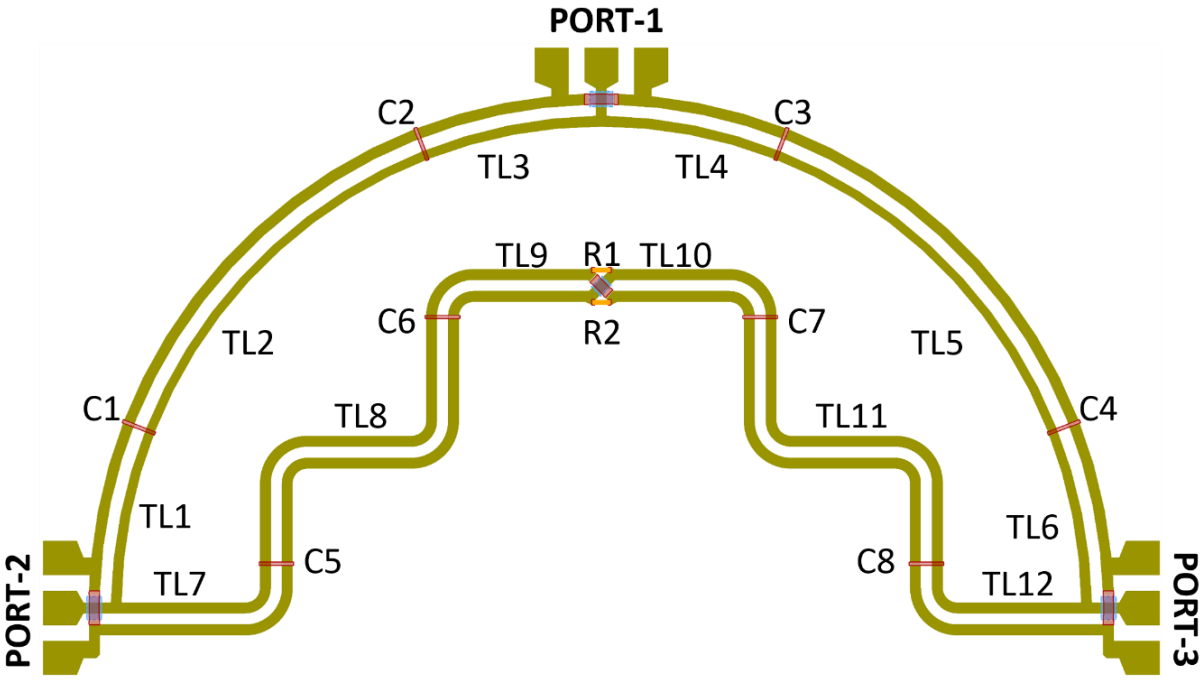


Figure 3.25 Layout image of the proposed ring power divider with component names

Table 3.2 Layout dimensions for components of the proposed CPW Offset Divider

Component Name	Width (µm)	Gap (µm)	Length (µm)	Component Name	Width (µm)	Gap (µm)	Length (µm)
TL1	26	40	536	**TL12**	30	36	550
TL2	26	40	1195	**C1**	26	40	10
TL3	26	40	536	**C2**	26	40	10
TL4	26	40	1195	**C3**	26	40	10
TL5	26	40	124	**C4**	26	40	10
TL6	26	40	536	**C5**	30	36	10
TL7	26	40	550	**C6**	30	36	10
TL8	26	40	1151	**C7**	30	36	10
TL9	30	36	550	**C8**	30	36	10
TL10	30	36	550	**R1**	12	-	40
TL11	30	36	1151	**R2**	12	-	40

3D EM simulation results of designed divider are shown in Figure 3.26. Insertion loss of the proposed divider is better than 0.7 dB in the operation frequency band (8 -12 GHz). Input return loss is lower than 16.1 dB and output return losses are less than 18dB. Isolations of output ports are higher than 23 dB in operation frequency band. Despite the miniaturization

efforts in the design stage, divider performance was not compromised when compared to simulation results of standard ring power dividers.

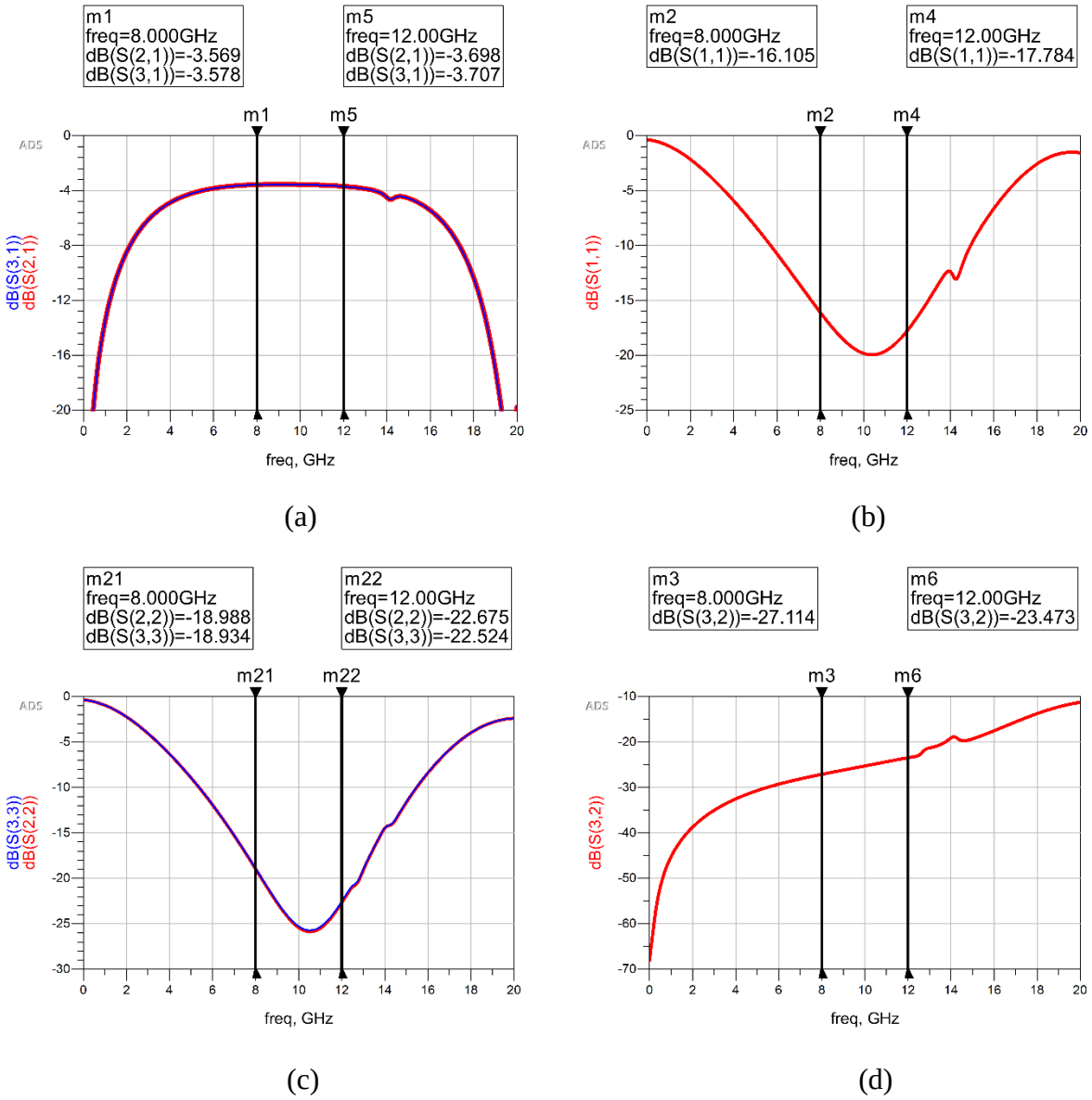


Figure 3.26 Simulation results of the designed ring power divider

a) Insertion losses b) Input return loss c) Output return losses d) Isolation of output ports

3.2.3. S-Parameters Measurements and Comparison of the Measurements with Simulation Results

In this section, S-parameters measurement results of the designed ring power divider and comparison of the measurement results with simulation results are presented. Microscope image of a fabricated ring power divider is seen in Figure 3.27.

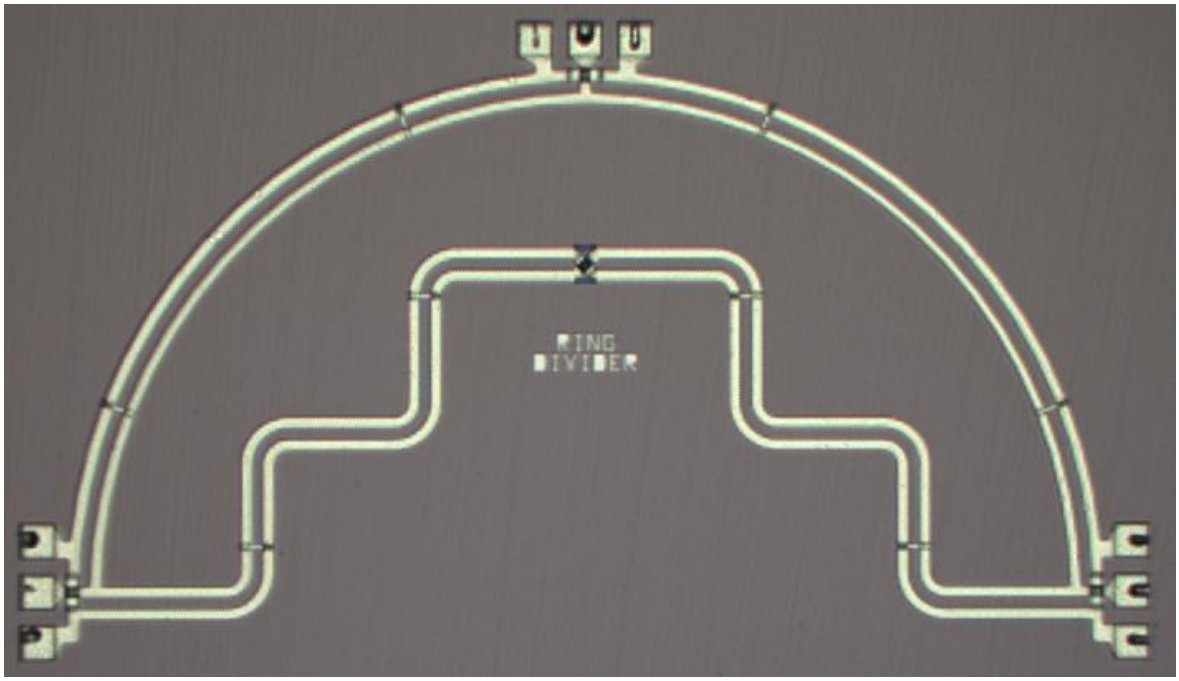
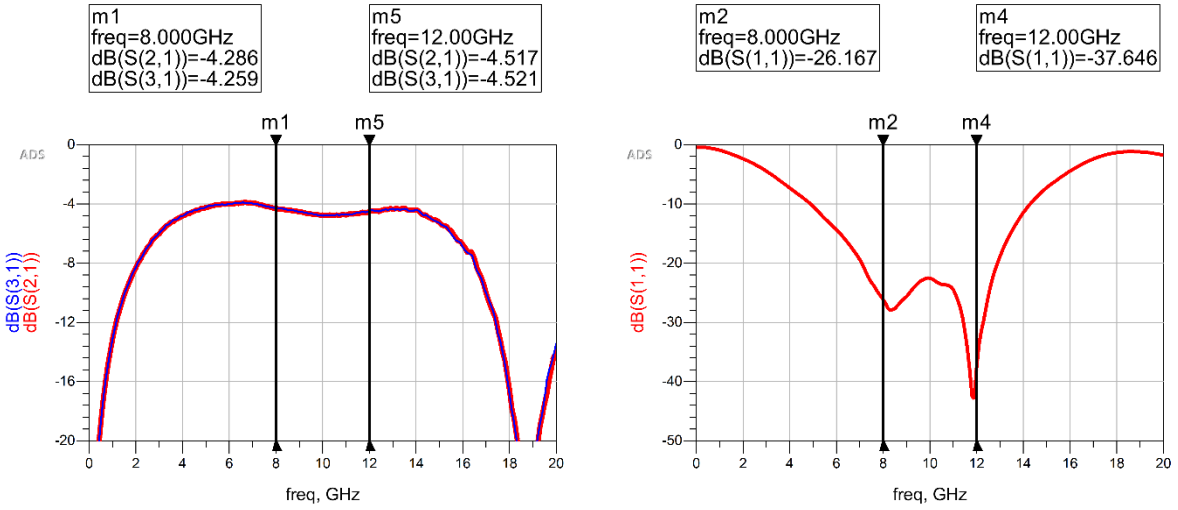
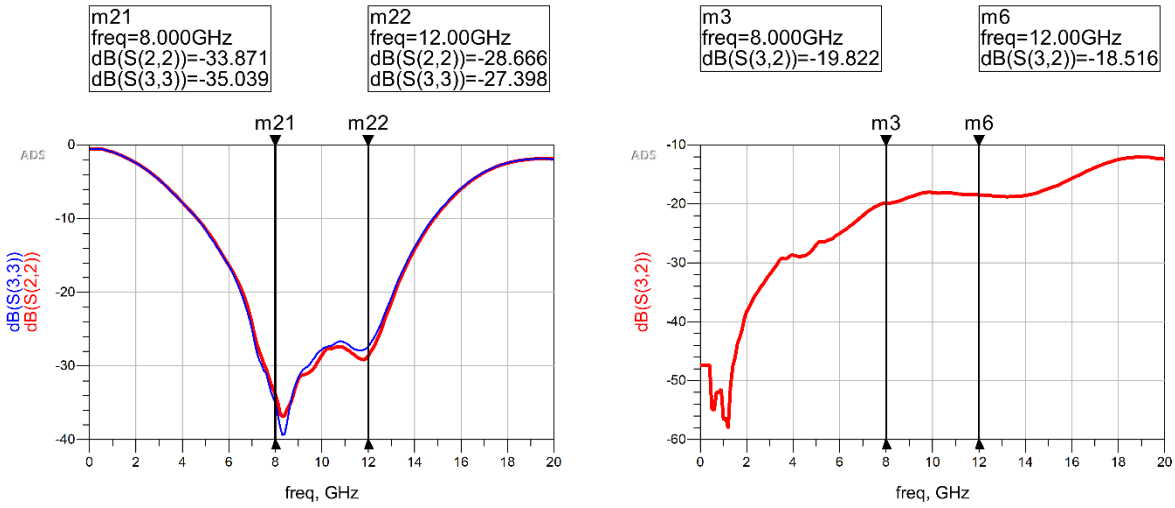


Figure 3.27 Microscope image of the fabricated ring power divider

3-port on-wafer small-signal measurements are performed with Rohde-Schwarz ZVA40 vector network analyzer. Port-1 is input port of the measured divider. Port-2 and Port-3 are designated as output, same with the convention followed in previous sections. Measurement results of fabricated ring power divider are demonstrated in Figure 3.28.



(a) (b)



(c) (d)

Figure 3.28 Measurement results of the fabricated ring power divider

a) Insertion losses b) Input return loss c) Output return losses d) Isolation of output ports

Comparisons of the simulation and measurement results for the designed and fabricated ring power divider are shown in Figure 3.29. Red lines represent the simulation results and blue lines represent the measurement results of the ring power divider. Input and output return losses and isolation of output ports are quite similar at the whole frequency band. However, measurement results of the insertion losses slightly drop at the center frequency (10 GHz) because of the variation introduced by the fabrication process and coupled line simulations. Thickness of the 240 nm thick insulator nitride layer may slightly vary among different fabrication runs. Due to this deviation, desired thickness levels can rarely be precisely obtained. This leads to different capacitance densities for the metal-insulator-metal capacitors used at the fabricated ring power divider, than the considered capacitance density in design.

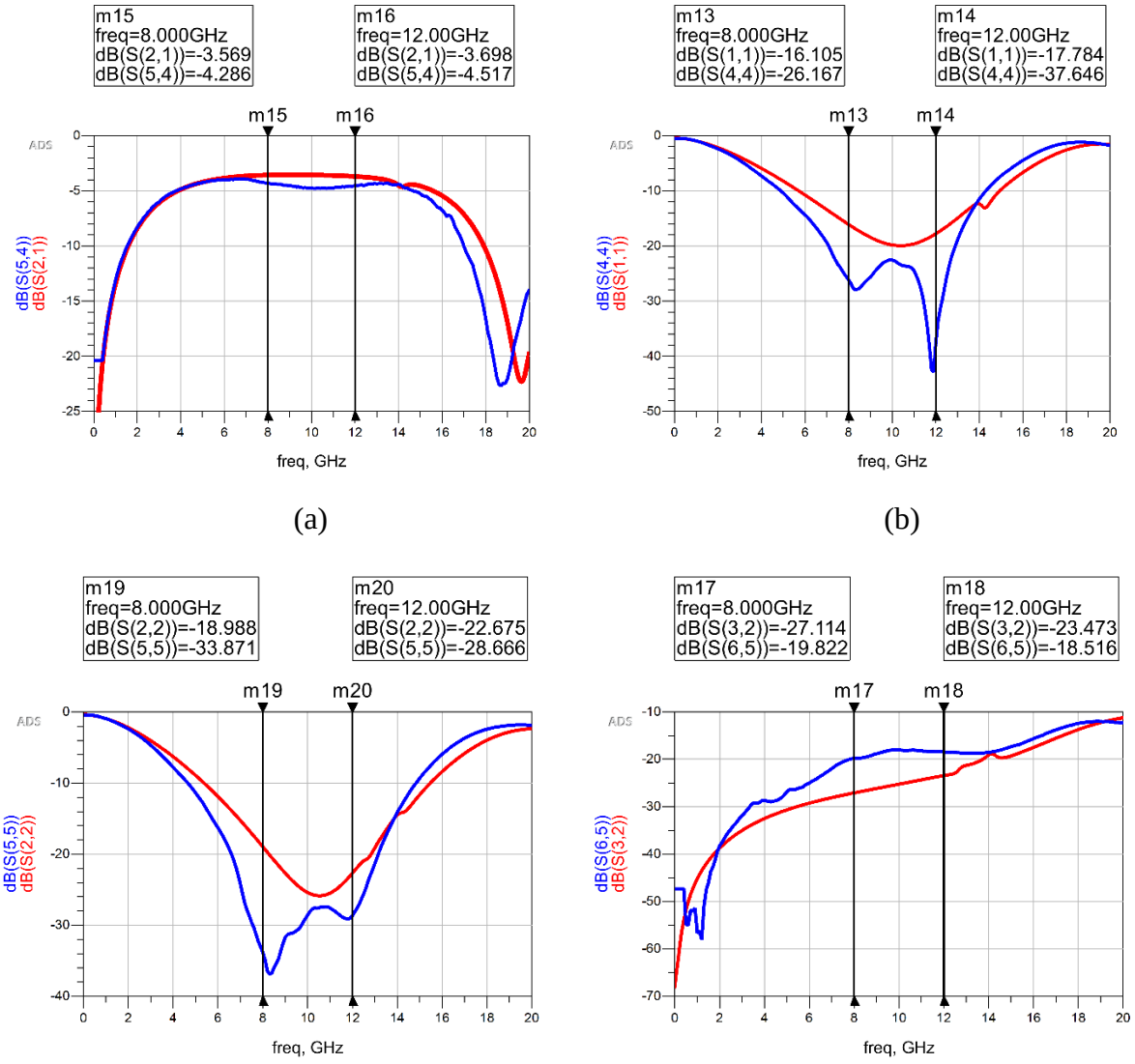


Figure 3.29 Simulation results and Measurement results of the ring power divider
a) Insertion losses b) Input return loss c) output return losses d) Isolation of output ports

3.3. Phase Shifted Wilkinson Power Divider

Wilkinson power dividers are one of the most widely used divider types in RF microwave circuits [23], [24]. Wilkinson power dividers are preferred in RF applications due to their high isolations and low insertion losses [25]. Simplified layout of a three-way Wilkinson power divider is shown in Figure 3.30. In this chapter of the thesis, analysis, design and measurements of an improved CPW Wilkinson power divider are presented. Reflection losses at the output ports of the 3-way divider are improved and phase difference between

the ports are introduced by adding transmission line sections at the end of the output ports of the three-way WPD.

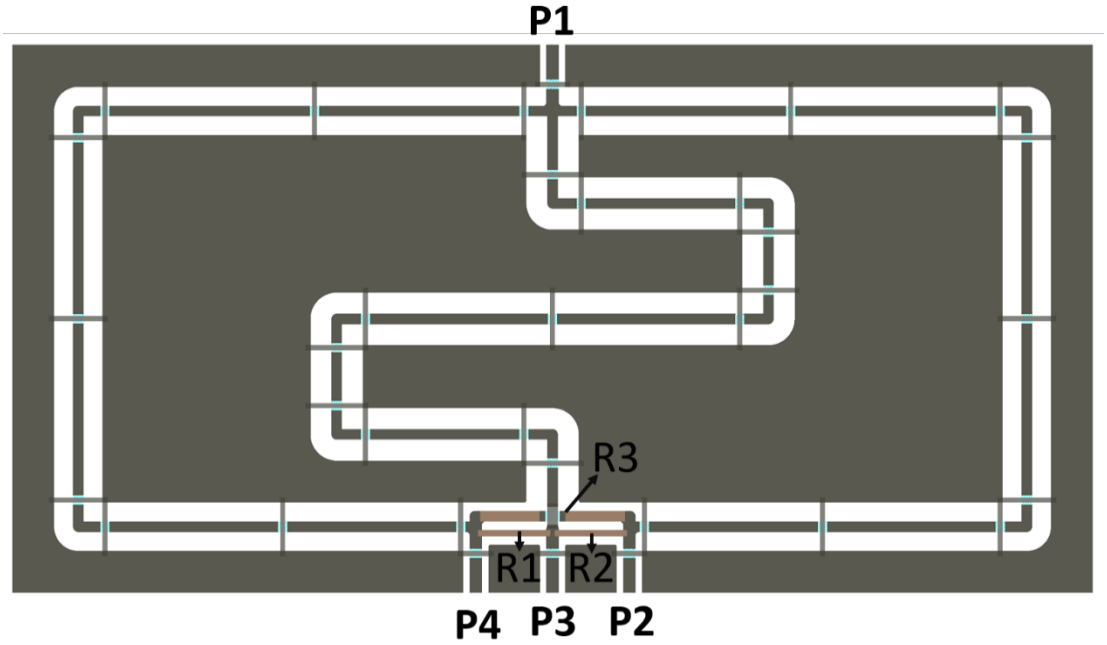


Figure 3.30 Simplified layout of the Wilkinson power divider

3.3.1. Analysis of the Phase Shifted Wilkinson Power Divider

In this part, theoretical analysis of the three-way phase shifted WPD is provided. Function of the phase shift at the output ports are explained and simulation results of a phase shifted Wilkinson power divider design with ideal circuit elements are demonstrated.

Incident waves to output ports of the three-way Wilkinson divider should be arranged as shown in the vector diagram in Figure 3.31, so that the reflections coming from the identical amplifiers (or any RF block, for that matter), which will be almost equal in amplitude and phase, will destructively interfere and cancel out each other. Port names at the Figure 3.31 are specified according to Figure 3.30. Due to the presence of three output ports, phase shift between reflected waves at output ports of the Wilkinson power divider should be 120^0 for the best reflection cancellation which is explained in more detail in Chapter 3.1.1. Therefore, taking Port-2 as the reference port, reflected signals coming to Port-3 and Port-4 should have

120^0 and 240^0 phase delays respectively, enhancing the return loss figures of any network connected to the output ports.

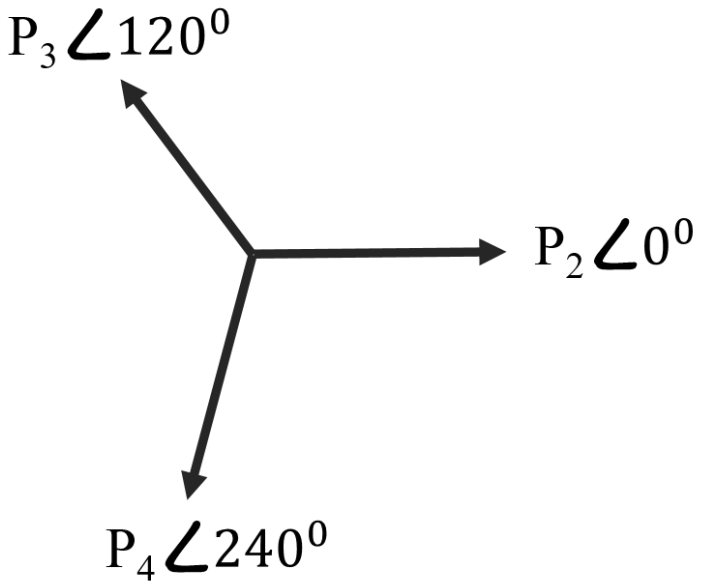


Figure 3.31 Relative phase of reflections from output ports

As evident from even-mode and odd-mode analyses of the Wilkinson power divider, characteristic impedances of transmission lines at the branches and resistors between output ports for three-way CPW Wilkinson power divider are calculated as in equations (3.30) and (3.31) below.

$$Z_L = Z_0\sqrt{3} \cong 86.6\ \Omega \tag{3.30}$$

$$R = 3Z_0 = 150\ \Omega \tag{3.31}$$

where Z_L represents the characteristic impedance of transmission lines at the branches and R is the value of the resistors between output ports.

Since all ports of the proposed Wilkinson power divider and the following blocks are matched to 50 Ω system impedance, phase delays are realized by adding 50 Ω transmission lines at the end of the output ports. Therefore, input and output term impedances in simulations are chosen as 50 Ω.

An ideal phase shifted Wilkinson power divider is designed around the frequency of 10 GHz, using ideal lumped components. Values of the component parameters are determined by the listed equations above. Schematic view of three-way phase shifted Wilkinson power divider with ideal lumped elements is shown in Figure 3.32.

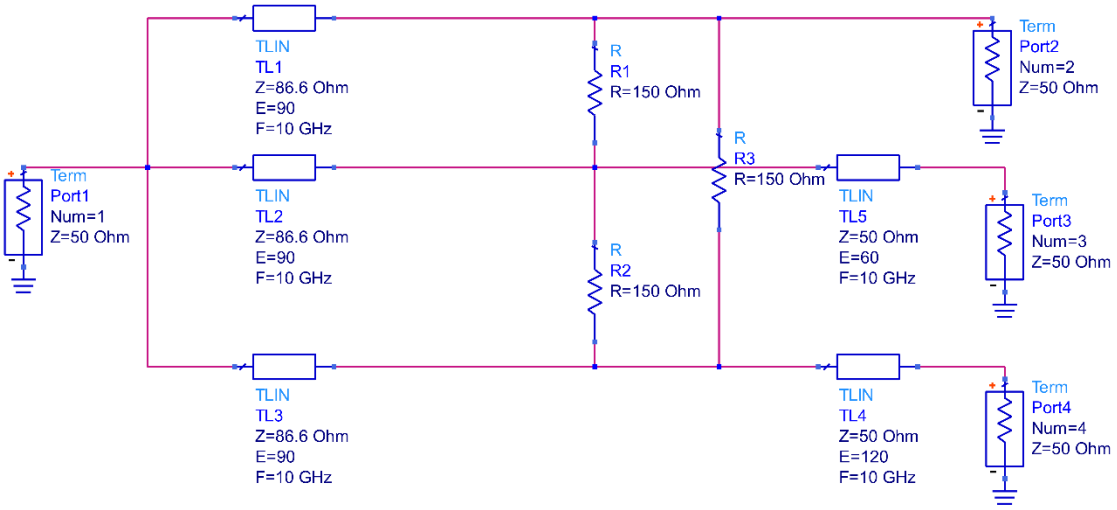


Figure 3.32 Schematic view of the ideal three-way phase shifted WPD

Port-1 is input port, whereas the Port-2, Port-3 and Port-4 are output ports of the three-way phase shifted WPD that is given in Figure 3.32. Simulation results for designed Wilkinson power divider at the 4 GHz - 16 GHz frequency band with ideal circuit elements are seen in Figure 3.33. Phases of the transmission coefficients for the individual branches, insertion losses, input and output port reflections and isolations between output ports are given in figures below. For the Figure 3.33c, red curve (S11) represents the input return loss, other lines represent return losses of the output ports.

Insertion losses of the ports are identical since the ideal lossless transmission lines are used and the design is perfectly symmetric in this schematic pre-design stage. It is important to note that these values are bound to change due to the real-world implementation losses, EM couplings, discontinuities and inevitable imperfections in the layout design phase of the divider.

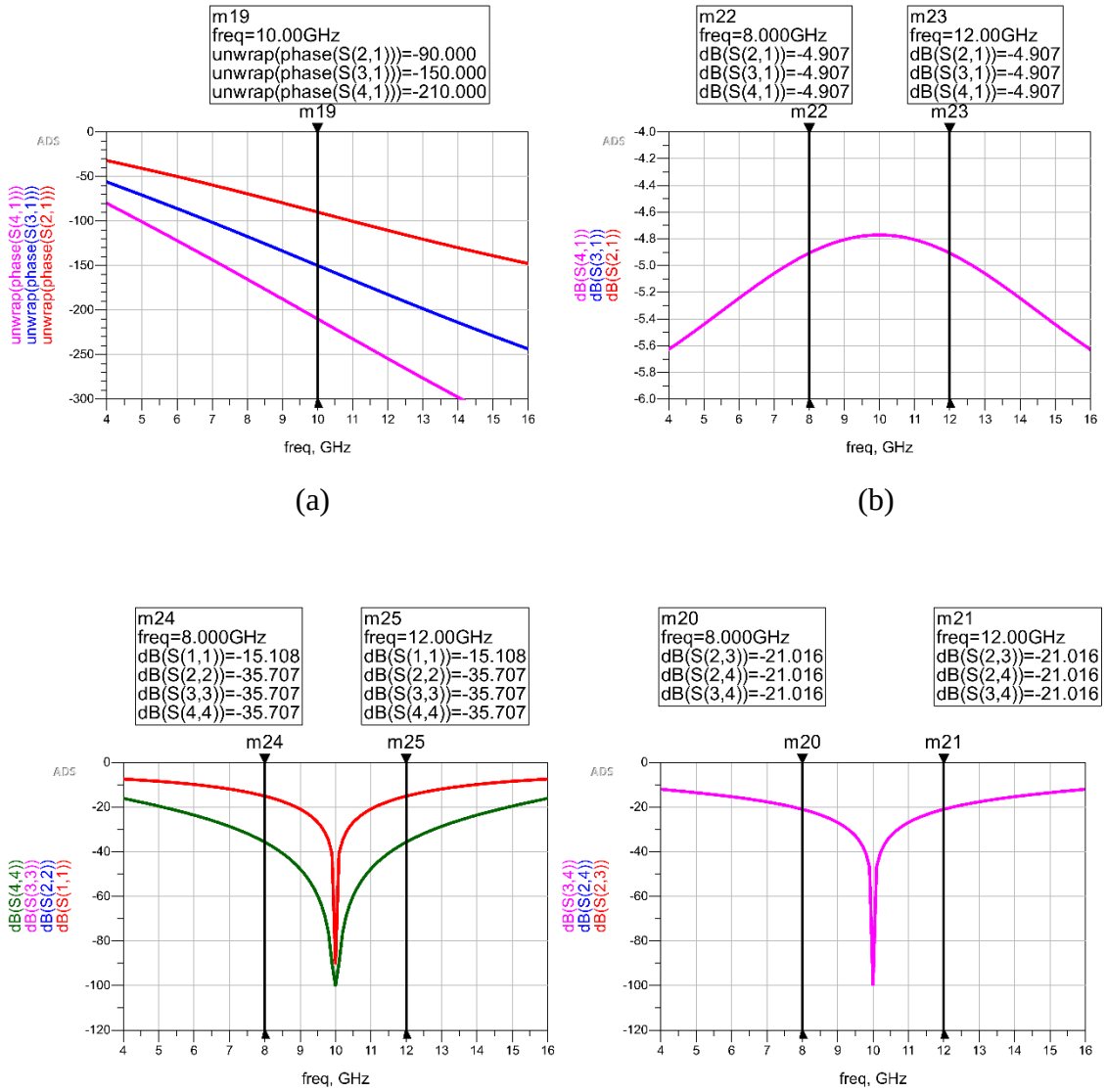


Figure 3.33 Simulation results of the ideal three-way phase shifted Wilkinson power divider

a) Phases b) Insertion losses c) Input and output return losses d) Isolations of output ports

3.3.2. Design Process and Simulation Results of Phase Shifted Wilkinson Power Divider

In this section, design techniques and EM simulation results of the proposed three-way phase shifted Wilkinson power divider in coplanar waveguide technology are presented. Layout view of the designed CPW Wilkinson power divider is seen in Figure 3.34. Overall size is 2.25 mm x 5.20 mm. Rectangular footprint area of the design is approximately 11.7 mm^2.

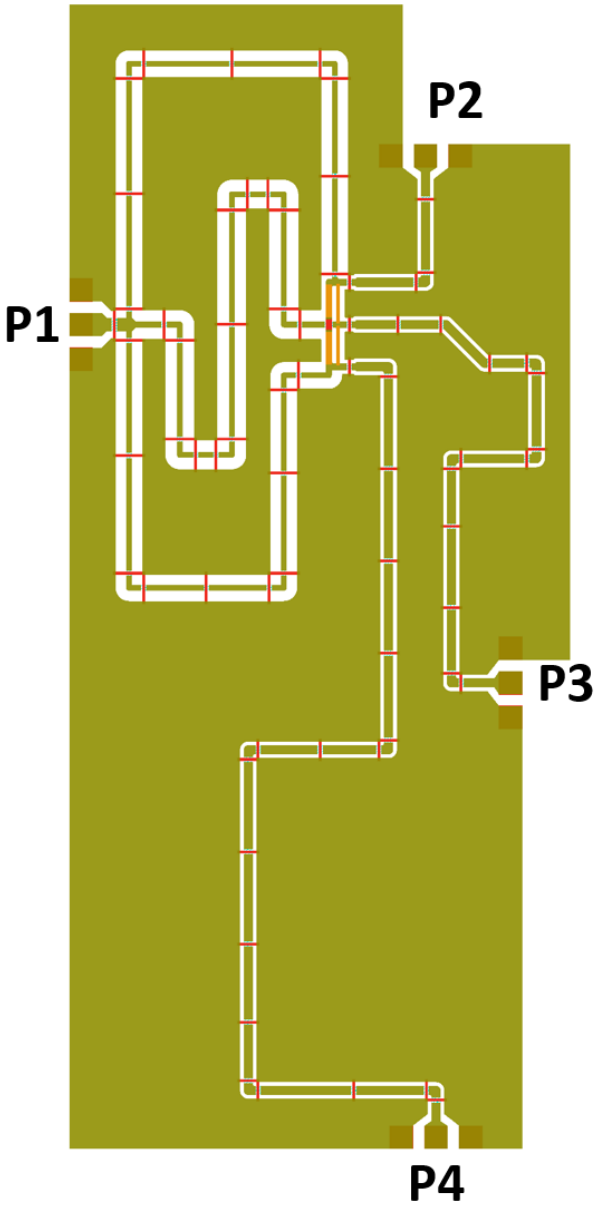


Figure 3.34 Layout view of the designed phase shifted Wilkinson power divider - 2.25 mm x 5.20 mm

Individual layout sections of the designed divider are denoted in ADS schematic view at Figure 3.35. Dimensions of the circuit components for the designed CPW three-way Wilkinson power divider are given in Table 3.3.

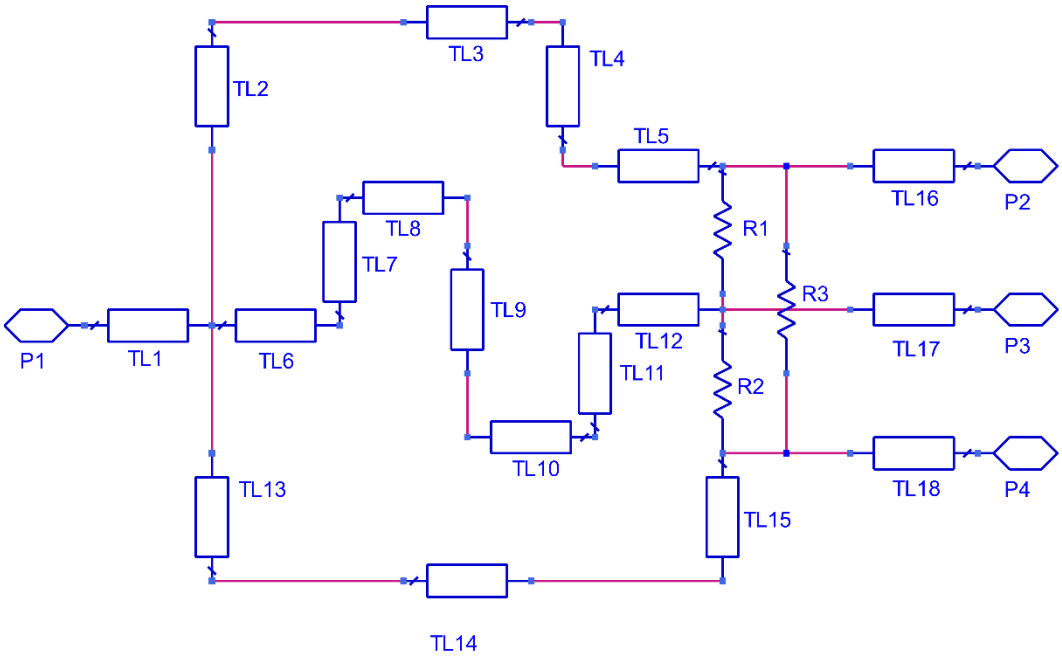


Figure 3.35 Schematic view of the designed Wilkinson power divider with component names

Table 3.3 Layout dimensions of individual components for the proposed CPW phase shifted three-way Wilkinson power divider

Component Name	Width (µm)	Gap (µm)	Length (µm)	Component Name	Width (µm)	Gap (µm)	Length (µm)
TL1	60	30	258	**TL11**	25	50	522
TL2	25	45	1147	**TL12**	25	50	217
TL3	25	45	665	**TL13**	25	45	1123
TL4	25	45	920	**TL14**	25	45	888
TL5	25	45	187	**TL15**	25	45	965
TL6	25	50	217	**TL16**	40	16	929
TL7	25	50	522	**TL17**	40	16	2890
TL8	25	50	210	**TL18**	40	16	4966
TL9	25	50	1028	**R1-R2**	15	-	150
TL10	25	50	210	**R3**	25	-	2x122

EM simulation results of the full layout are seen in Figure 3.36. Phase difference between output ports are approximately 120^0 at the center frequency of 10 GHz. Insertion losses of the proposed divider are less than 1.2 dB at the center frequency. At the end of frequency band (12 GHz), insertion loss becomes approximately 1.6 dB at Port-4, which extended with the longest (120^0) transmission line. Input return loss is lower than 11 dB and output return

losses are better than 20 dB, whereas isolations of the output ports are better than 20 dB in the operation frequency band of 8 to 12 GHz. Corresponding to a fractional bandwidth of %40, results can be considered as a wideband design.

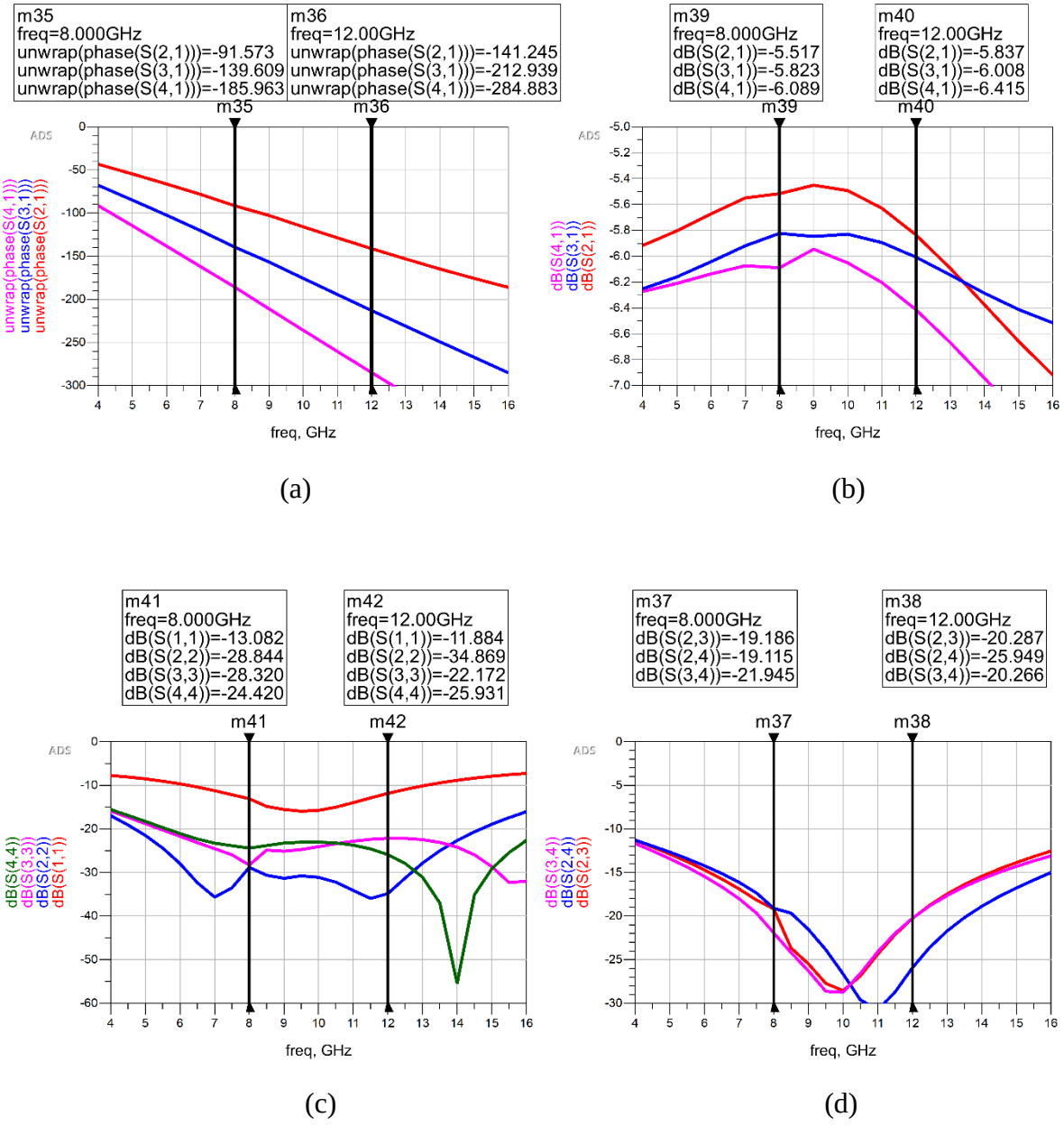


Figure 3.36 Simulation results of the designed Wilkinson power divider

a) Phases b) Insertion losses c) Input and output return losses d) Isolations of output ports

3.3.3. S-Parameter Measurement Results and Comparison of the Measurement Results with Simulation Results

In this section, S-parameter measurement result of the fabricated Wilkinson power divider is presented and compared with the simulation results. Microscope image of a fabricated power divider is seen in Figure 3.37.

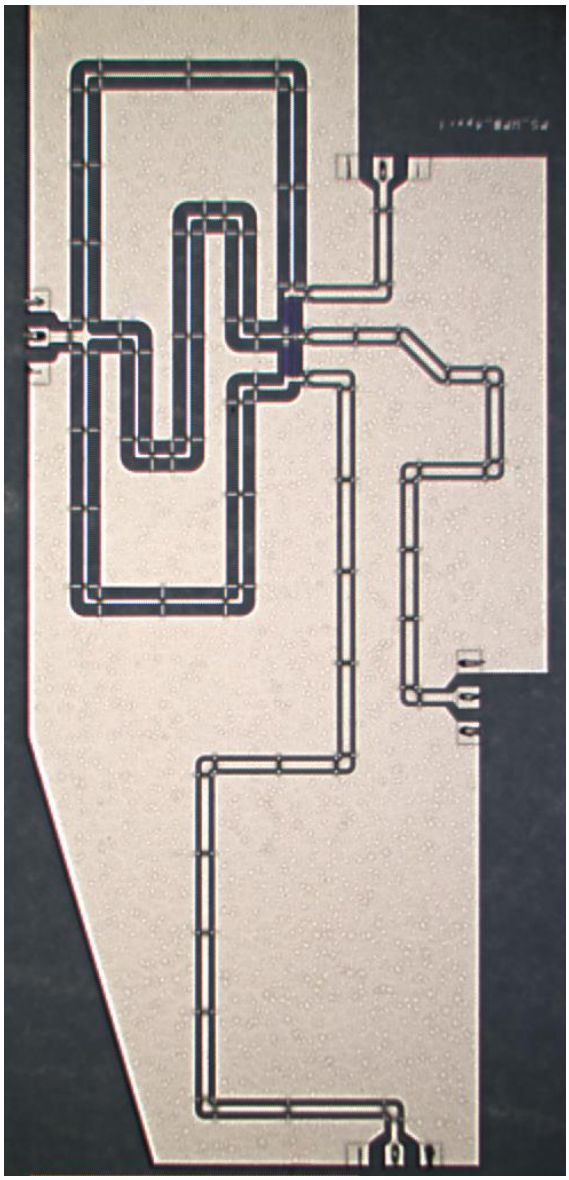


Figure 3.37 Microscope image of the fabricated CPW phase shifted Wilkinson Power Divider

Input port and three output ports are designed to face different directions and placed orthogonally in order to allow 4-port on-wafer measurements, as seen in Figure 3.37. Measurement results of the fabricated Wilkinson power divider are demonstrated in Figure

3.38. Phase differences of the ports are demonstrated in Figure 3.38a. Insertion losses are given in Figure 3.38b. Red curve at Figure 3.38c is represents the input return loss, other curves show the return losses of output ports. In Figure 3.38d, isolations of the output ports are presented.

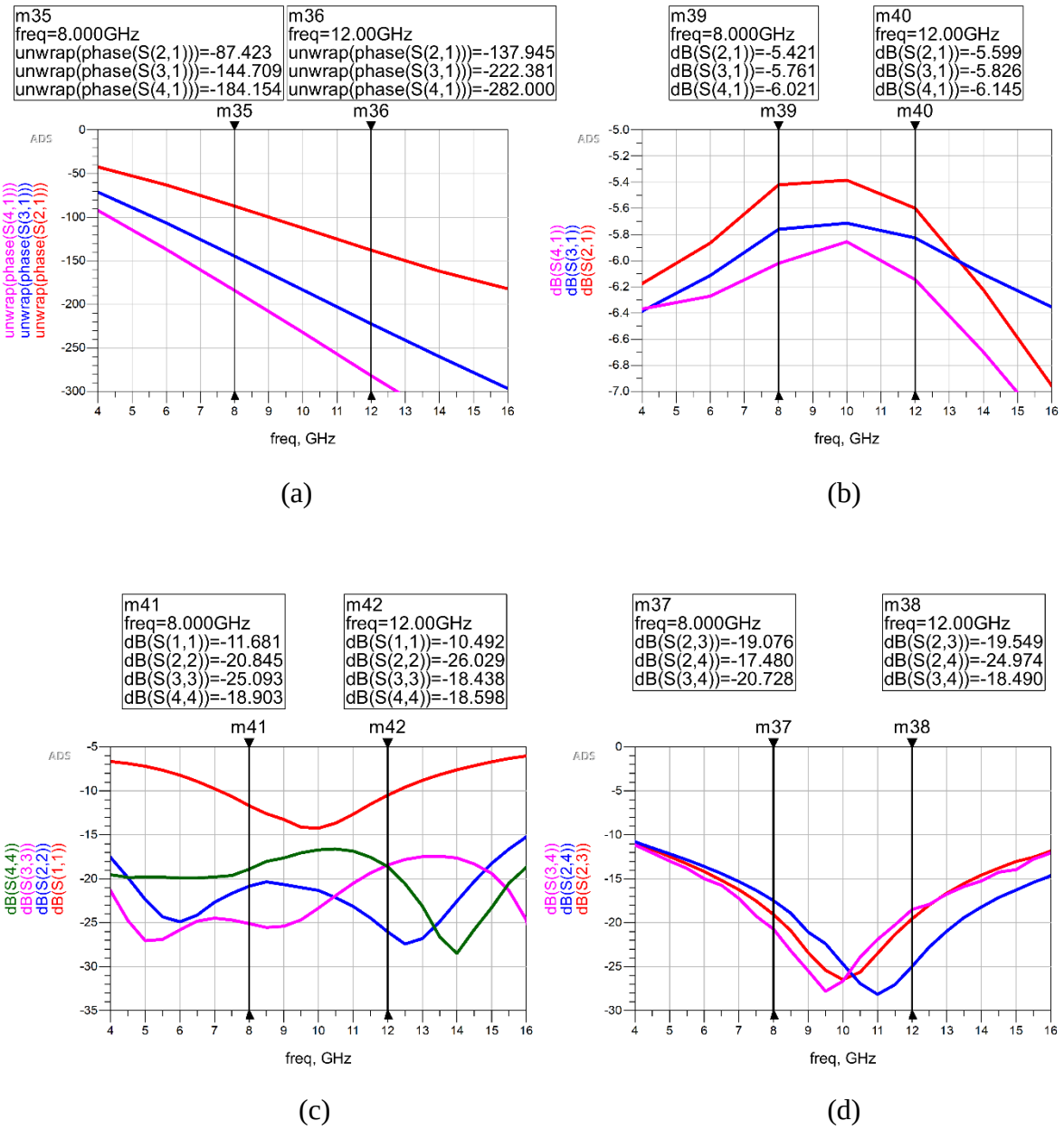
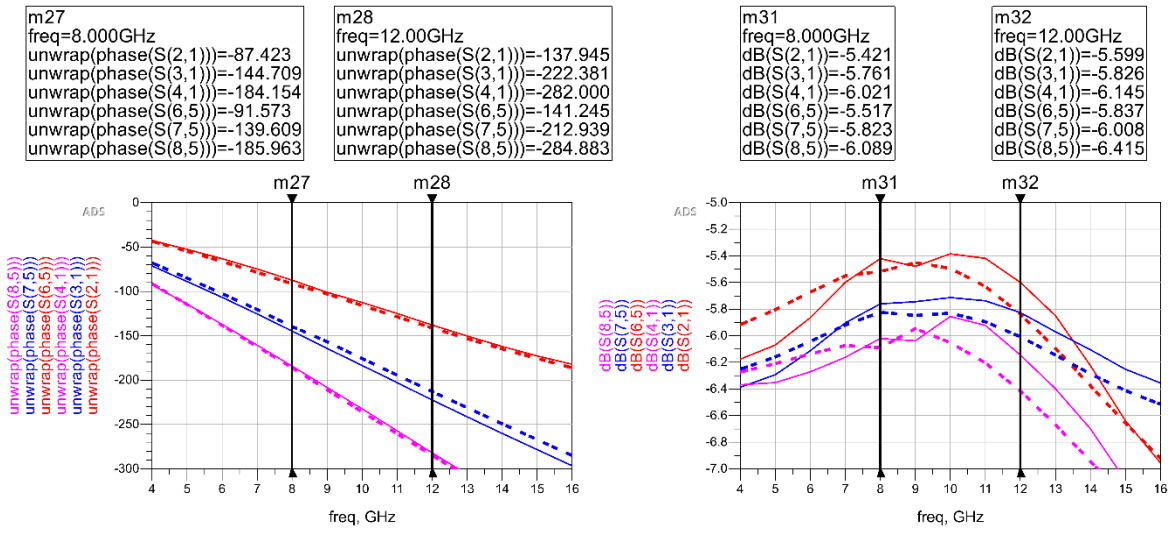


Figure 3.38 Measurement results of the fabricated phase shifted Wilkinson power divider a) Phases b) Insertion losses c) Input and output return losses d) Isolations of output ports

Phase differences between output ports at the center frequency are approximately 60^0 and 120^0 respectively. Measurement results of the insertion losses are better than 1.4 dB throughout the operation frequency band for the longest branch and better than 0.8 dB for

the shortest branch. Input return loss is better than 10 dB and output return losses are better than 17 dB in the whole frequency band. Also, isolations of the output ports are lower than 20 dB as seen in Figure 3.38. Comparisons of the simulation and measurement results for the designed and fabricated Wilkinson power divider are seen in Figure 3.39. Dotted lines represent simulation results and solid lines are on-wafer measurement results. Measurement results and simulation results are in good agreement, indicating accurate EM substrate definition and simulation settings.



(a) (b)

(c) (d)

Figure 3.39 Simulation results and measurement results of the Wilkinson power divider a) Phases b) Insertion losses c) Input and output return losses d) Isolations of output ports

The designed phase shifted divider/combiner is shown in Figure 3.37 in a typical balanced MMIC power amplifier application. In this configuration, amplifier blocks are driven with RF signals 60^0 apart in phase. Phases of the amplified RF signals are then equalized at the output power combining stage with the opposite phase differences, as demonstrated in the functional block diagram shown in Figure 3.40.

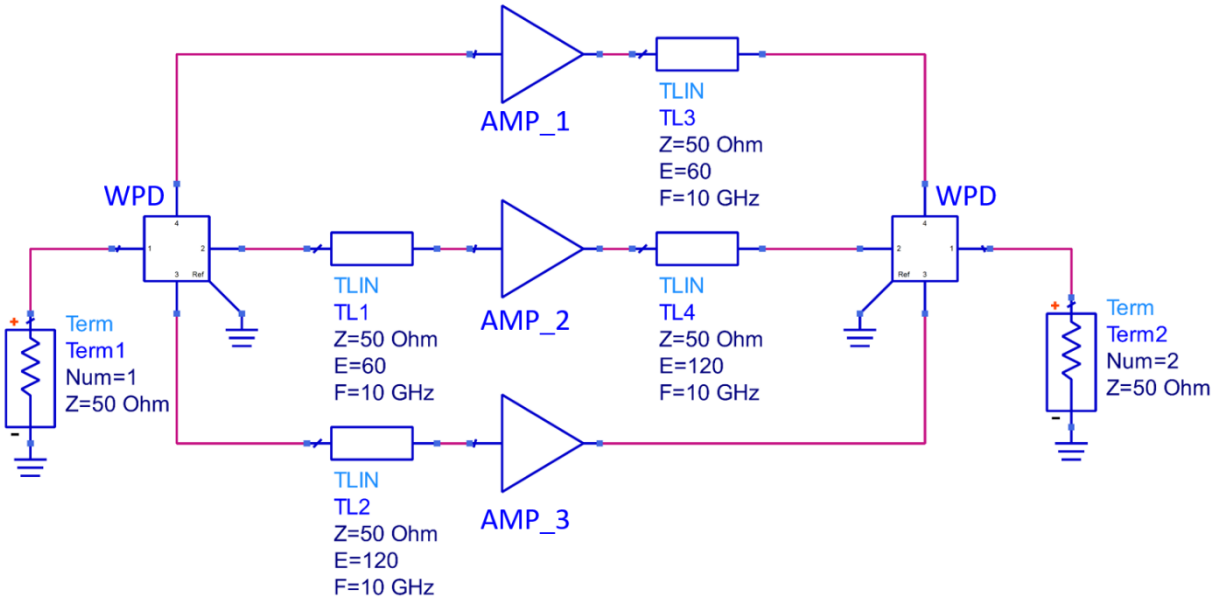


Figure 3.40 Functional block diagram of the balanced MMIC power amplifier design implemented with phase shifted Wilkinson power divider/combiners

In order to implement this circuit topology, the mirrored (with respect to x-axis) version of the designed three-way phase shifted Wilkinson divider/combiner is utilized. Phase shifts at the divider stage are undone at the combining stage by the mirrored combiner, so that the RF signals at the output combine in-phase. Example usage of this divider in a MMIC design is shown in the layout given in Figure 3.41.

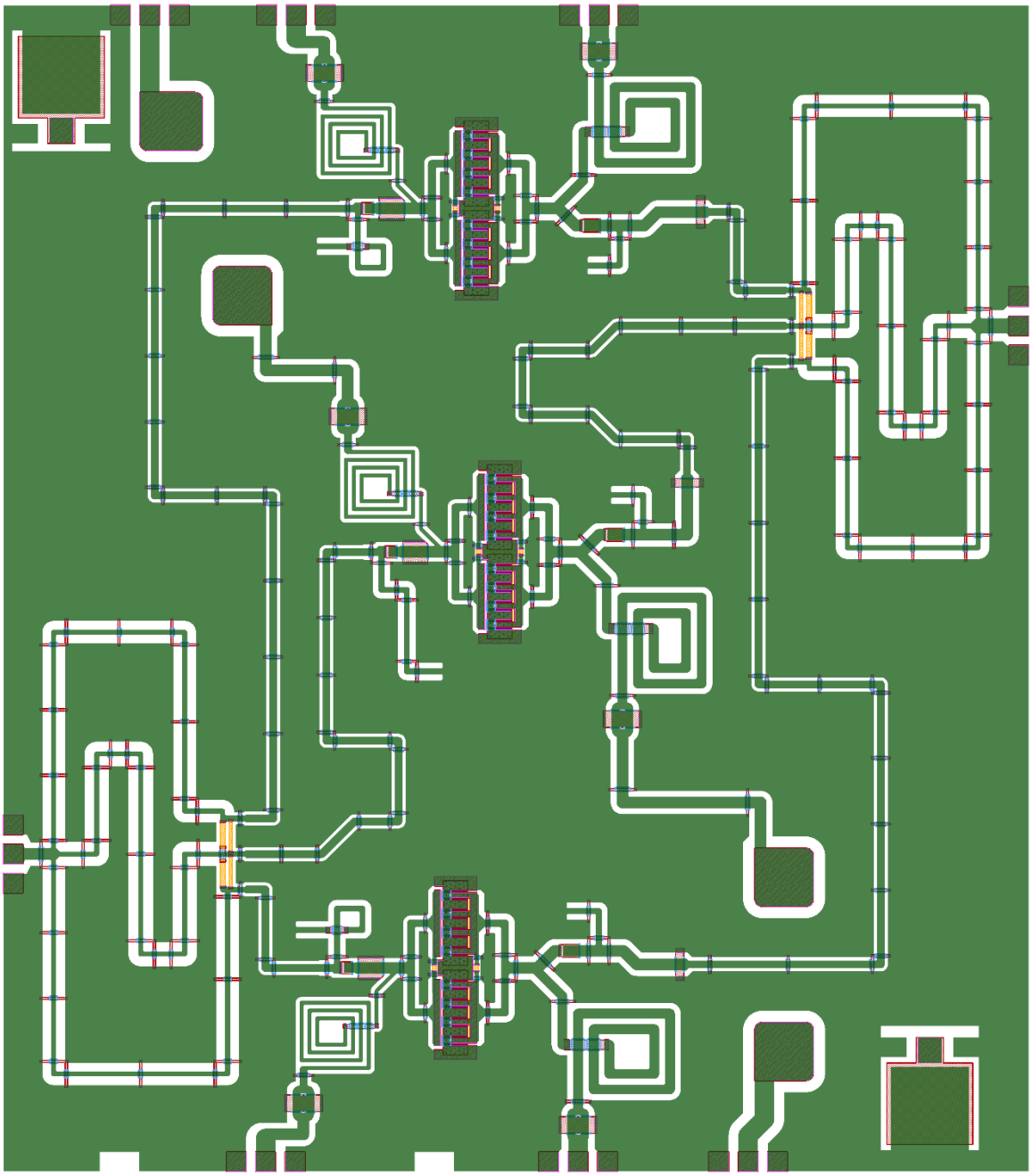


Figure 3.41 MMIC design with three-way CPW phase shifted Wilkinson power divider/combiner

3.4. Corporate Power Divider

Footprint area of a design is one of the most important parameters for the GaN based RF microwave circuits since unit die area for high-end GaN processes are quite expensive when compared to other semiconductor technologies such as CMOS and GaAs, as well as PCB implementations [26]. Because of the high implementation cost, RF circuit designers prefer to miniaturize their circuits as much as possible. For this reason, designers try to combine output and input matching circuits with the power divider/combiner networks. Therefore, corporate power divider structures are widely utilized for power combining/division and matching in RF circuits, avoiding a significant amount of passive circuitry. In this section, a four-way *X*-band corporate power divider is analyzed, designed and measurements results of fabricated test structures are presented. This power divider is designed for combining output powers of 4 HEMTs at the output stage of a power amplifier MMIC. Also, it functions as output cluster matching network and transistor biasing network. General circuit view of the four-way corporate power divider/combiner is illustrated in Figure 3.42.

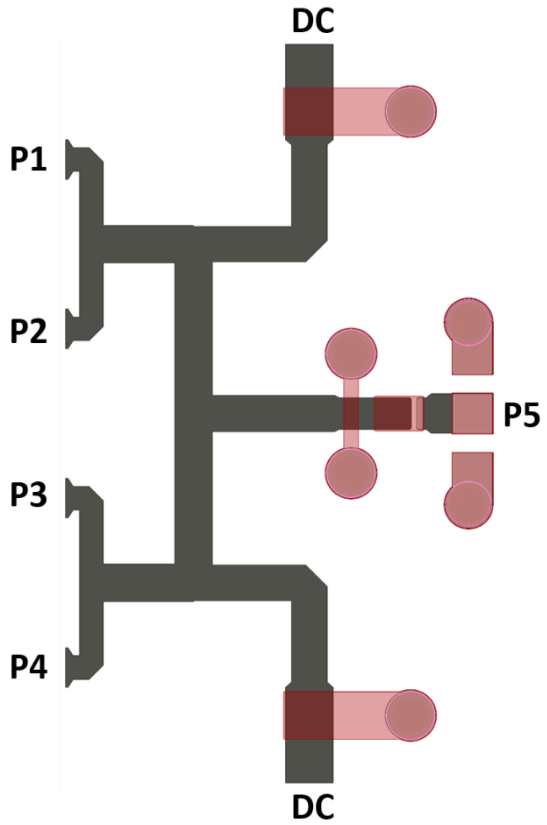


Figure 3.42 General Circuit View of the corporate power divider

P1, P2, P3 and P4 are connected to outputs of the HEMTs, P5 is the output port of the whole MMIC where all of the RF output power is combined. Ports marked as "DC" are the on-wafer biasing pads where transistor DC voltages are supplied through bond wires or DC bias probes.

3.4.1. Analysis of the Corporate Power Divider

In this section, three main aspects of the four-way corporate power divider is analyzed: RF-DC isolations, impedance matching techniques and DC block capacitors. Simulation results of the design regarding these analyses are also presented.

Firstly, there should be sufficiently high isolation between DC ports of the network and the RF portion of the circuit. Therefore, RF signal doesn't leak through the DC bias lines. RF isolation in the operation frequency band is crucial to prevent feedback loops between the outputs and inputs of transistors. Amplified RF signals can easily find paths/loops with gains more than unity, resulting in unwanted and uncontrolled oscillations in circuit. Additionally, lack of sufficient isolation between the RF and DC portions of the circuit means that any external modification of the circuit after the DC ports (wire bonding, packaging, addition of discrete off-chip elements) will also affect the RF portion of the circuit, altering the carefully engineered load impedances presented by the designed matching network. Therefore, one of the most significant aspects while designing the corporate power divider is the DC port design and isolation.

Ideally, DC bias networks contain an RF choke inductor which would present very high impedance to the circuit at high frequencies, thus having negligible effect on impedance matching in the operation frequency band. However, DC networks cannot include large on-chip inductors since they occupy lots of valuable die area, thus are skipped in design due to the size restrictions. Therefore, DC bias network affects impedance matching. For this reason, this part of the circuit is incorporated into the matching network design as a shunt matching element which acts like a shorted transmission line stub.

Designed DC bias network is given in Figure 3.43. Port-1 is the RF and Port-2 is the DC_{in}. DC bias network is designed using series transmission line and a shunt capacitor with adjustable ground via distance in order to constitute a shunt L-C band stop filter network. A

number of the shunt capacitors with larger sizes can be added for better isolation of lower frequencies than the designed frequency band (8 GHz – 12 GHz). However, these extra elements are usually added out of chip as discrete on-board or on-probe capacitors.

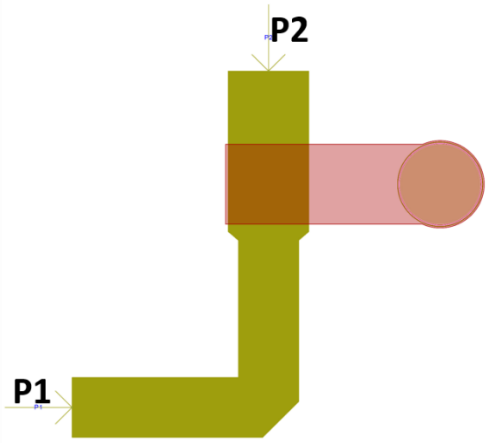


Figure 3.43 Layout view of the designed DC network

Simulation results of the layout design at Figure 3.43 are seen in Figure 3.44. Isolation between DC port and RF ports is better than -21dB at desired frequency band. Therefore, any addition to the circuit after the DC pads (probes, bond wires, off-chip bias elements, etc.) does not affect the input/output port impedances of the corporate power divider in the desired frequency band and RF signal does not leak through the DC bias network.

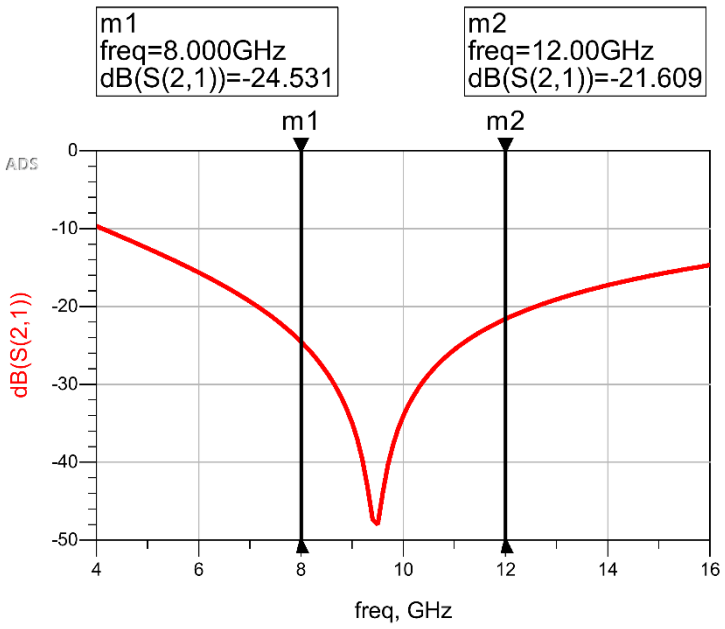


Figure 3.44 Simulation Results of the designed DC bias Network

DC bias passes through the RF circuit to output of the transistors. DC block capacitor is used near the output of the power divider in RF line as series capacitor. Therefore, DC voltage is blocked at the output of the power divider. Also, because of the area concern, this capacitor that is shown in Figure 3.45 cannot be large enough to be seen as short circuit in operation frequency band. Therefore, a small capacitor is used which is incorporated as part of matching circuit. RF and DC routes are marked in Figure 3.45.

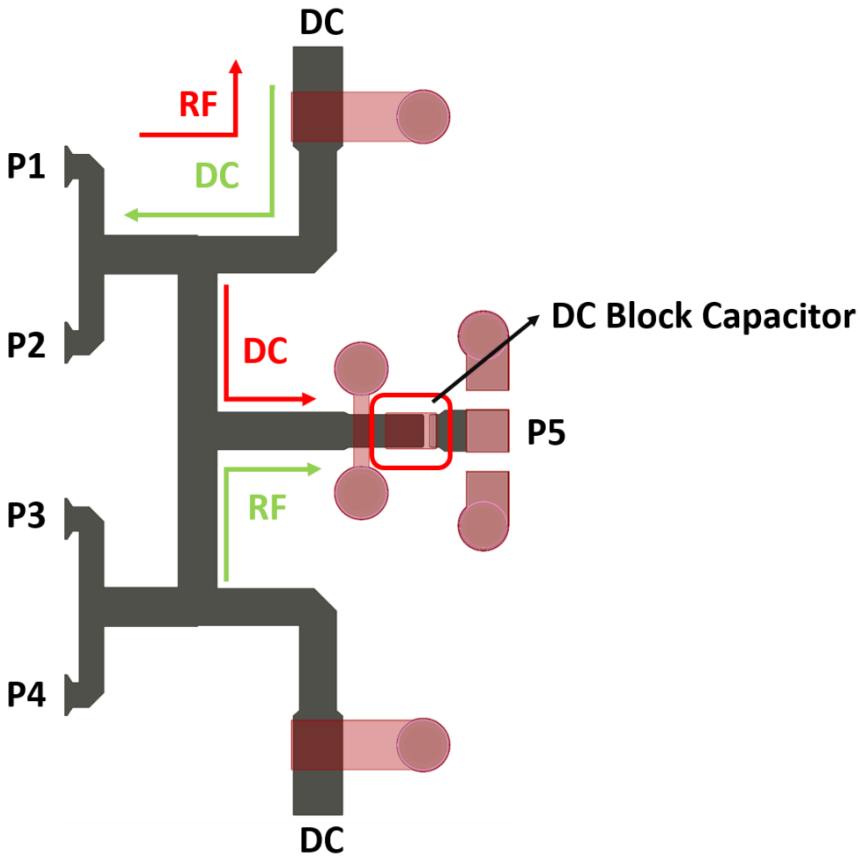


Figure 3.45 DC block capacitor at the output of the designed power divider with DC & RF current routes marked

There are four input ports that are shown in Figure 3.45. These input ports should have the same forward transmission phase in order for ideal in-phase power combination at branches to occur with minimal loss. Because of the asymmetry between inner input ports (P2-P3) and outer input ports (P1-P4), forward transmission phases for input ports are slightly different. Therefore, phase difference of the outer and inner input ports are tried to be minimized as much as possible at the design stage. As part of this effort, distance between

the RF signal paths at the input ports of the divider and DC bias lines are maintained by implementing DC bias network as far away from the branches as possible. This way, undesirable coupling effects and asymmetry caused by the DC bias line are prevented.

Simulation results of the phase difference between outer and inner input ports of the final design is given in Figure 3.46. Phase differences between input ports are lower than 5^0 in desired frequency band.

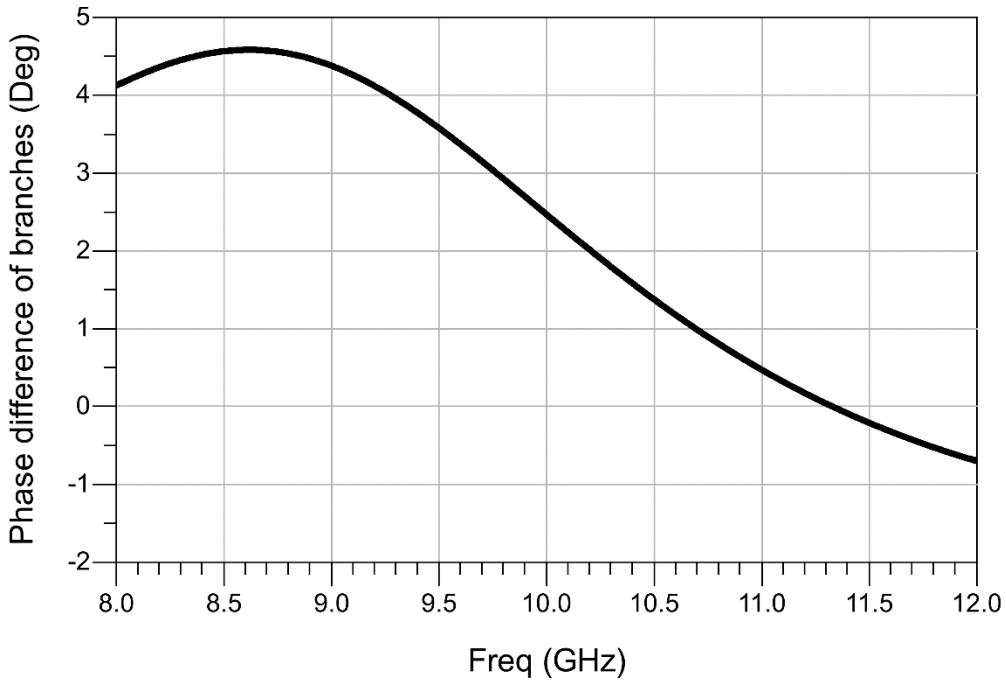


Figure 3.46 Phase Difference between inner and outer input ports of the designed corporate power divider

Arguably the most important thing at the design stage is the even-mode input impedances of the corporate power divider. Ideal load impedances that should be presented to transistor outputs for obtaining high output power are experimentally determined by transistor load-pull measurements, since devices operate in non-linear large-signal regime at high power/compression levels. Input impedances of the corporate power divider should be matched excellently to the conjugate of these load impedances for obtaining high output power from MMIC. In the tradeoff between low loss and wide band for the corporate power divider design, it is preferred to use as few components as possible in order to achieve a low loss matching network.

3.4.2. Design Process and Simulation Results of Corporate Power Divider

In this section, layout design and 3D EM simulation results of the proposed corporate divider in microstrip (MS) technology are presented. Layout view of the designed corporate power divider is seen in Figure 3.47.

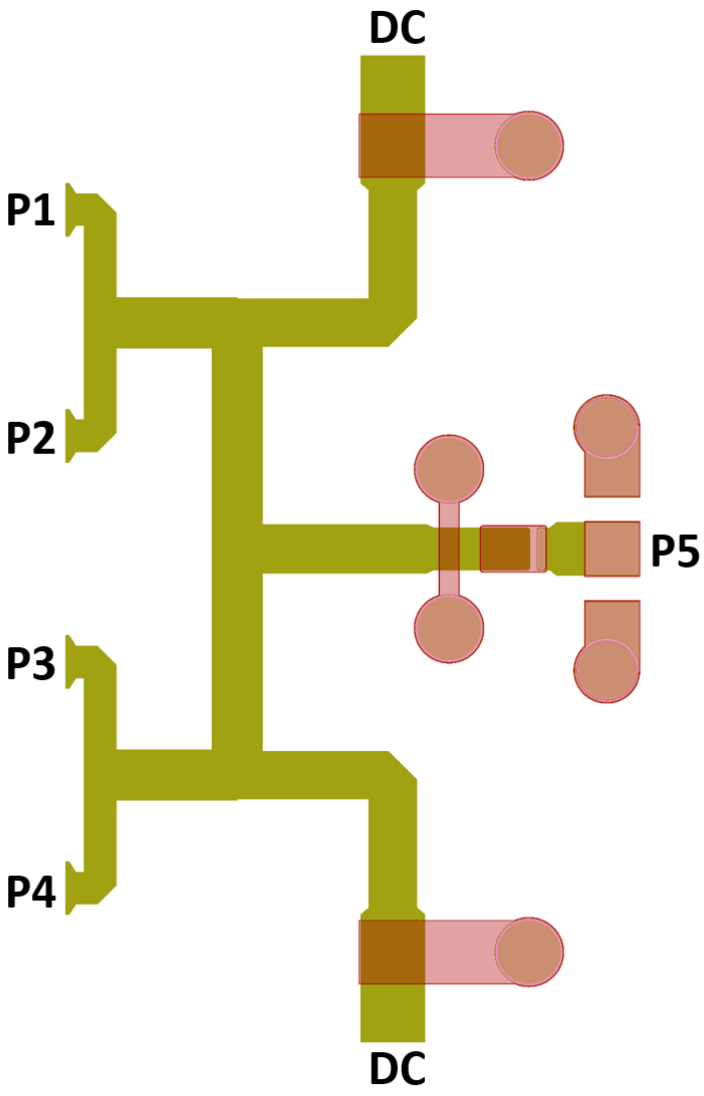


Figure 3.47 Layout view of the designed corporate power divider

Overall size of the designed corporate power divider is 1.00 mm x 1.80 mm. Rectangular footprint area of the design is approximately 1.8 mm^2. 3D EM Simulation results of the designed divider are seen in Figure 3.48. Insertion loss is lower than 0.46 dB in desired frequency band. Impedances seen at inner and outer branches/input ports of the corporate

power divider are quite similar. These impedances correspond well to the proper load-pull impedances for the maximum output power of the MMIC. Phase difference between inner and outer input ports are given above Figure 3.46 for this design.

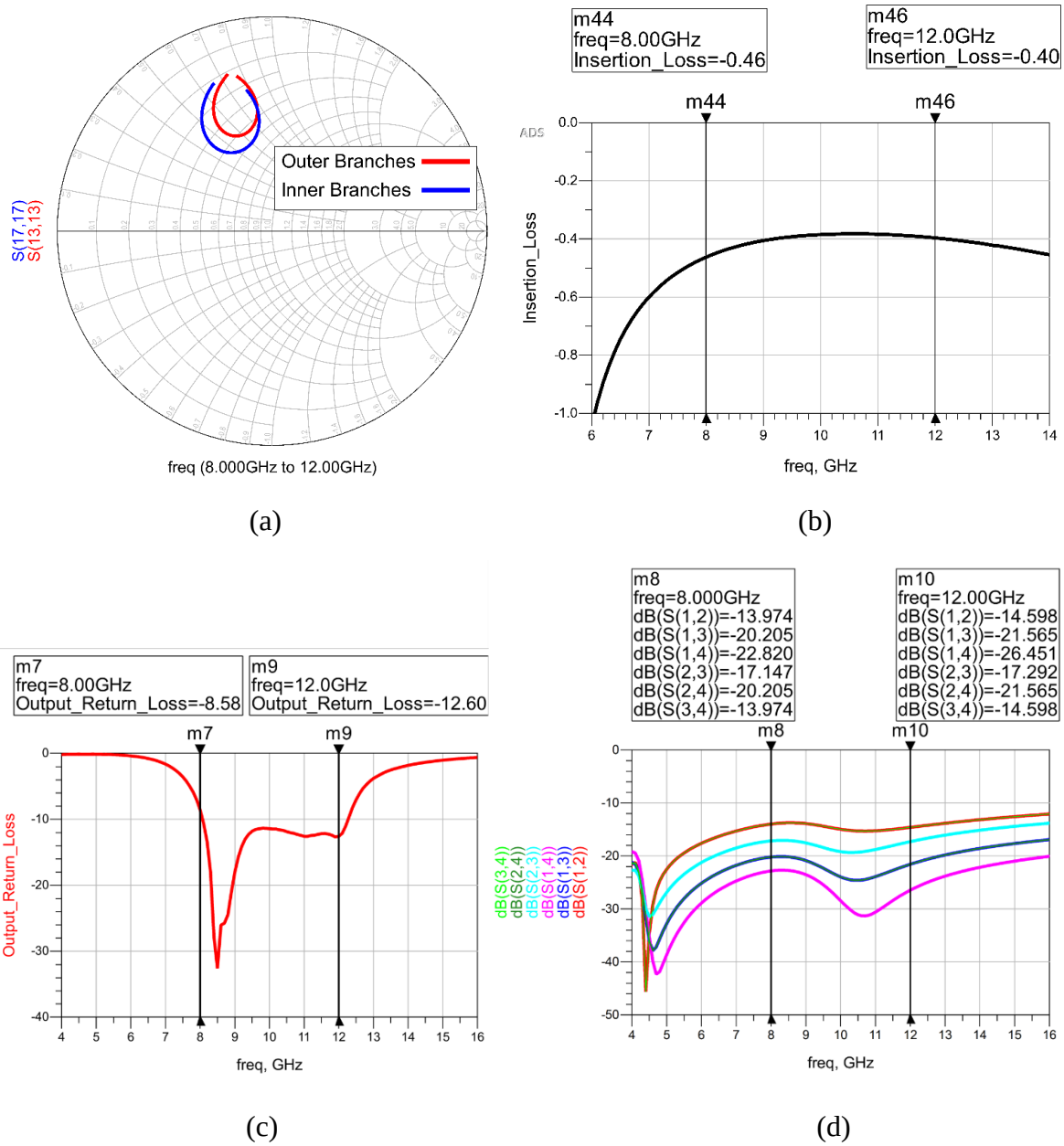


Figure 3.48 Simulation results of the designed corporate power divider

a) Impedances at inner and outer input port b) Insertion losses c) Output return loss

d) Isolations at output ports

Ideal circuit component equivalent of the designed divider is shown in ADS schematic as shown in Figure 3.49. Dimensions of the circuit components at the designed MS corporate power divider are given in Table 3.4.

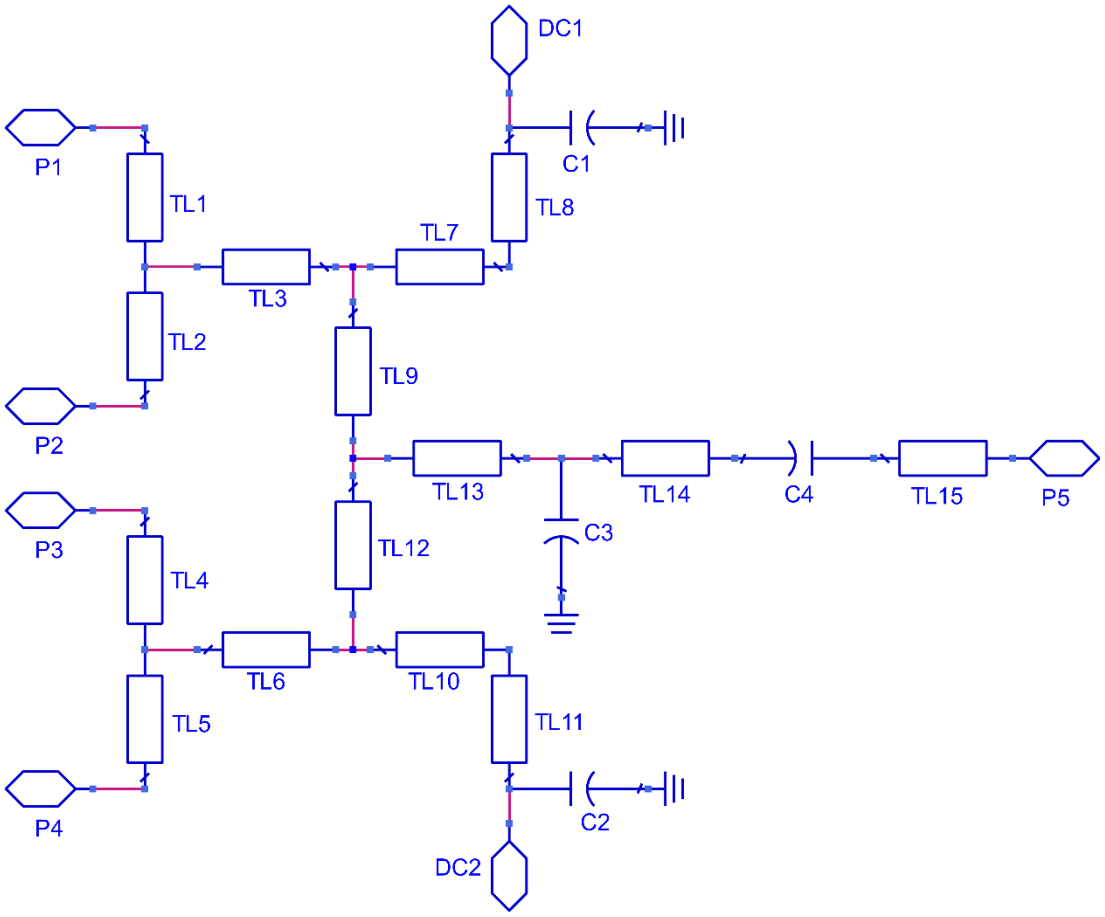


Figure 3.49 Schematic view of the designed corporate power divider with component names

Table 3.4 Dimensions of the components at the proposed MS corporate power divider

Component Name	Width (µm)	Length (µm)	Component Name	Width (µm)	Length (µm)
TL1	60	280	**TL10**	90	267
TL2	60	280	**TL11**	90	275
TL3	95	258	**TL12**	95	418
TL4	60	280	**TL13**	92	380
TL5	60	280	**TL14**	80	40
TL6	95	258	**TL15**	100	173
TL7	90	267	**C1-C2**	120	120
TL8	90	275	**C3**	80	37
TL9	95	418	**C4**	80	93

3.4.3. S-Parameter Measurement Results of the Corporate Power Divider Test Structures

In this section of thesis, S-parameter measurement results of the fabricated corporate power divider test structures are presented.

Two different type of test structures for corporate power dividers are fabricated. Probe positions at the input sides are different for these corporate power dividers. In this way, 2-port on-wafer measurements can be performed to examine the performance of fabricated structures. Two-port measurements are performed by terminating other input ports with 50Ω thin film resistors. Phase difference between inner and outer input ports, as well as the insertion losses can be determined with these S-parameter measurements. Microscope image of a fabricated MS corporate power dividers are seen in Figure 3.50.

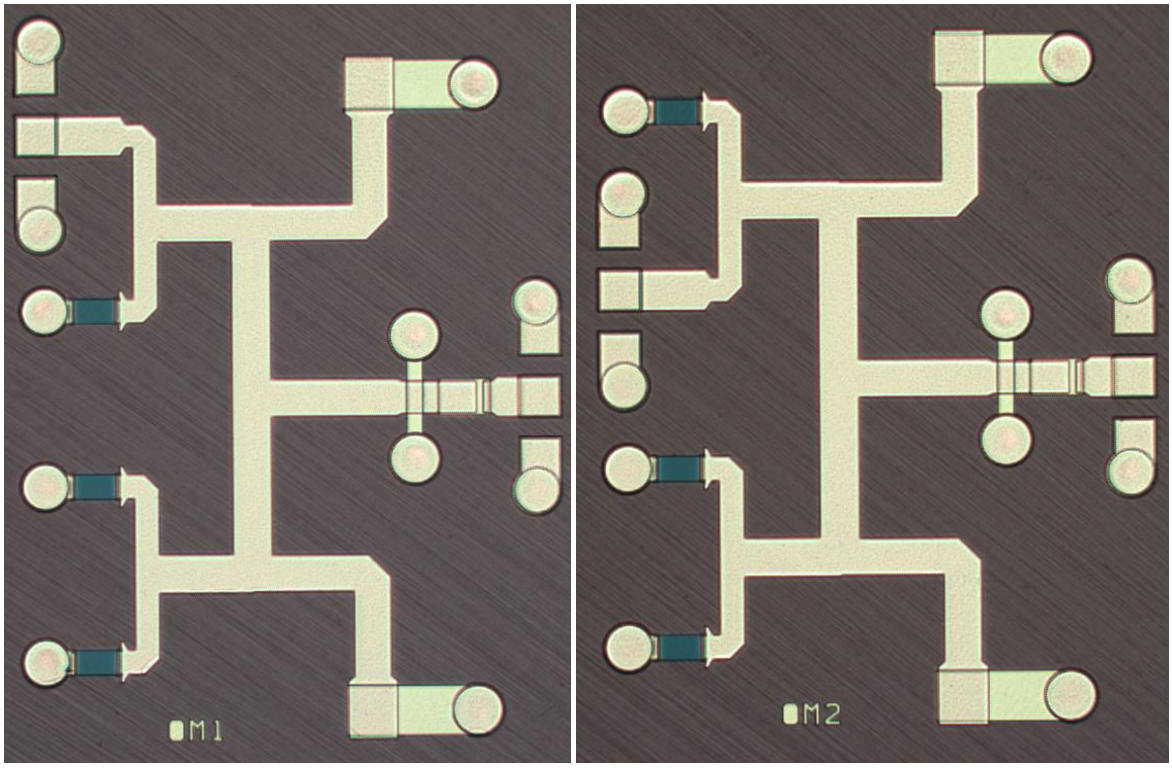


Figure 3.50 Microscope images of the fabricated MS corporate power dividers

Measurement results of the designed corporate power divider are demonstrated in Figure 3.51. Phase difference between outer and inner input port is demonstrated.

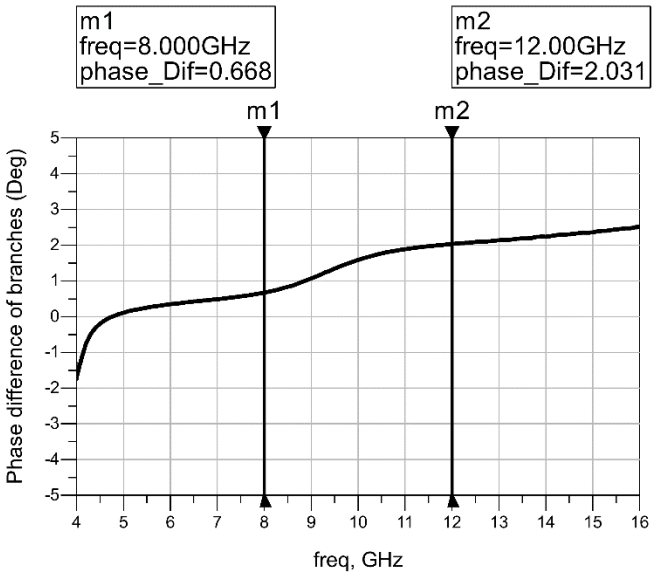


Figure 3.51 Measurement results of phase difference between the inner and outer input port

Microscope image of the fabricated MMIC that is constructed with corporate power divider which is analyzed above is shown in Figure 3.52. Detailed results (Design stages, S-parameter and power measurements) of this MMIC are presented in [27].

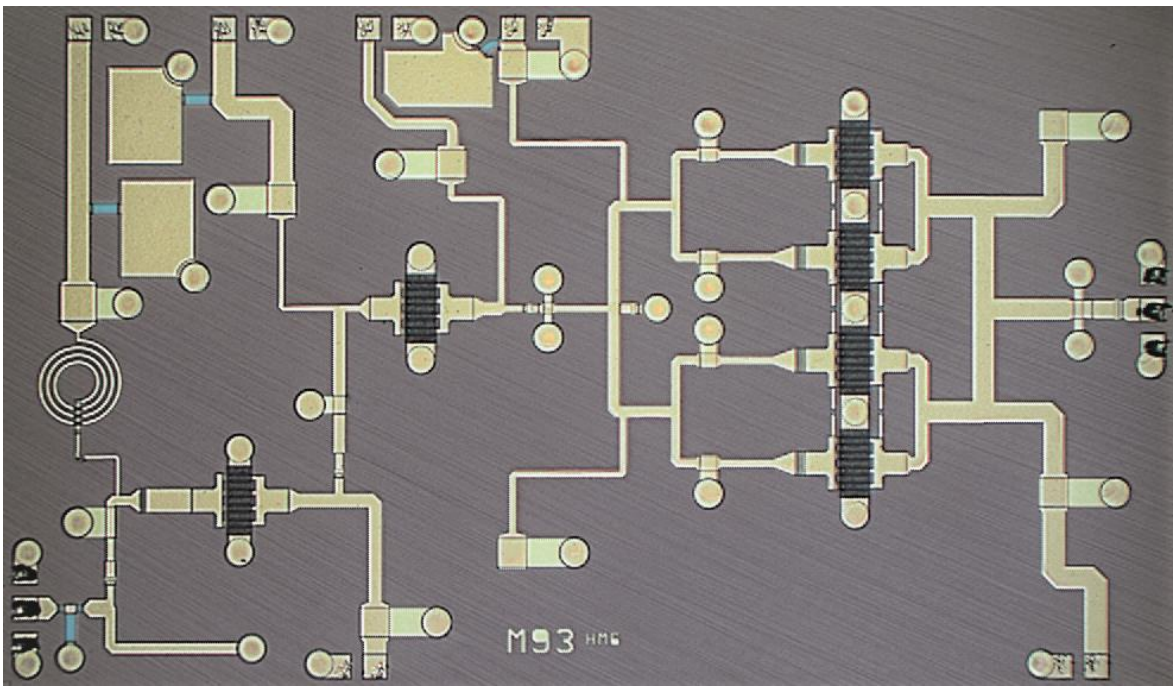


Figure 3.52 Microscope image of the fabricated MMIC with corporate power divider

4. CONCLUSION

In this thesis, four different SiC based power divider/combiner structures at *X*-band are analyzed, designed, fabricated and measured.

The miniaturized CPW offset-power divider/combiner structure is presented. Impedance analysis of the designed CPW offset-power divider/combiner is performed. Effective footprint of the designed four-way miniaturized offset-power divider is 2.2mm^2. Effective footprint is reduced approximately 55 percent for the designed offset divider by using miniaturization techniques that are the π-shaped structure methodology and meandering the transmission lines. Simulation results of the insertion losses for the output branches are lower than 1 dB at the center frequency (10 GHz). Phase shifts of reflections at the output ports are approximately $90^\circ \pm 5^\circ$. Isolations of the output ports are better than 9 dB, except the isolation between Port-4 and Port-5. Reflection of the input port is better than 10 dB in the 8 -12 GHz frequency band. Designed offset-power divider/combiner are connected back to back in order to evaluate performance of fabricated structures with 2 port measurements. Measurement results and simulation results are in good agreement, indicating accurate EM substrate definition and simulation settings.

Ring power divider/combiner is analyzed and designed regarding to even-odd mode conditions. Miniaturization techniques also are used at layout design stage of the ring power divider. Effective footprint of the designed two-way ring power divider is calculated as 4.4 mm^2. Effective area is reduced by approximately 72 percent compared to commercial ring power divider structures. Insertion loss of the designed divider is lower than 0.8 dB in the operation frequency band (8 -12 GHz). Input return loss is better than 16 dB and output return losses are less than 18 dB. Isolation of the output ports is better than 23 dB in the operation frequency bandwidth. Although miniaturization techniques are used at the layout design stage, performance of the designed miniaturized power divider keep up with simulation results of the commercial ring power dividers.

Phase Shifted WPD structure is presented. Function of phase shift at the output ports is explained. Phase shift is applied designed WPD to enhance return loss figures of any network that is connected to output ports. Effective footprint area of the proposed phase shifted three-way Wilkinson divider is approximately 11.2 mm^2. Measurement results of the phase

differences between output ports at the center frequency are approximately 120^0 and 240^0 respectively. insertion losses are better than 1.4 dB throughout the operation frequency band for the longest branch and better than 0.8 dB for the shortest branch. Input return loss is better than 10 dB and output return losses are better than 17 dB in the whole frequency band. Also, isolations of the output ports are lower than 20 dB. Simulation and measurement results are quite similar with each other at the desired frequency band.

Four-way *X*-band corporate power divider/combiner is analyzed. This power divider is designed to combine output powers of four HEMTs at the output stage of a power amplifier. Also, it functions as output cluster matching network and transistor biasing network. RF-DC isolations, impedance matching techniques and DC block capacitors are analyzed for the designed MS four-way corporate power divider/combiner structure. Overall size of the designed corporate power divider is approximately 1.8 mm^2. 3D EM Simulation results of insertion loss is lower than 0.46 dB in desired frequency band. Impedances seen at inner and outer branches/input ports of the corporate power divider are quite similar. These impedances correspond well to the proper load-pull impedances for the maximum output power of the power amplifier. Phase difference between inner and outer input ports are better than 5^0.

Summary of the proposed power divider combiner structures are shown in Table 4.1.

Table 4.1 Properties of the designed power divider/combiner structures

	offset-power divider	Ring power divider	PS Wilkinson power divider	Corporate power divider
# of output ports	4	2	3	4
Effective footprint	2.2mm^2	4.4 mm^2	11.2 mm^2	1.8 mm^2
Size reduction	55%	72%	-	-
Insertion losses	> -1 dB	> -0.8 dB	> -1.4 dB	> - 0.46 dB
Input Return Losses	> -12 dB	> -16 dB	> -10 dB	-
Output Return Losses	> -5 dB	> -18 dB	> -17 dB	> -9 dB
Isolations	> -9 dB	> -23 dB	> -20 dB	> -14 dB
Phase Differences	$90^\circ \pm 5^\circ$	0°	$120^\circ \pm 5^\circ$	0°

In addition, High power amplifiers are designed by using phase shifted Wilkinson power divider and corporate power divider. Layout view of the proposed high-power amplifiers MMICs are presented.

As a future work, high power amplifiers at *X*-band can be designed by using offset-power divider/combiner and ring power divider structures. Other type of the miniaturization techniques can be applied to minimize the effective footprint of the designed power dividers/combiners.

5. BIBLIOGRAPHY

[1] Pozar, D.M., "*Microwave Engineering"*, John Wiley and Sons, Inc., **1998**.

[2] Cohn, Seymour B., and Ralph Levy. "History of microwave passive components with particular attention to directional couplers." *IEEE Transactions on Microwave Theory and Techniques* 32.9, 1046-1054, **1984**.

[3] E. J. Wilkinson, "*An N-way hybrid power divider*," IEEE Transactions on Microwave Theory and Techniques, vol. 8, no. 1, pp. 116–118, **1960**.

[4] U. H. Gysel, "*A new N-way power divider/combiner suitable for high power applications*," in MTT-S International Microwave Symposium Digest, pp. 116–118, Palo Alton, CA, USA, May, **1975**.

[5] Marsh, S.P., "*MMIC power splitting and combining techniques"*, GEC Journal of Technology, **1997**.

[6] K. Song, Y. Fan and Y. Zhang, *"Eight-Way Substrate Integrated Waveguide Power Divider With Low Insertion Loss,"* in IEEE Transactions on Microwave Theory and Techniques, vol. 56, no. 6, pp. 1473-1477, June **2008**.

[7] C. W. Byeon and C. S. Park, *"Low-Loss Compact Millimeter-Wave Power Divider/Combiner for Phased Array Systems,"* in IEEE Microwave and Wireless Components Letters, vol. 29, no. 5, pp. 312-314, May **2019**.

[8] L. Chiu and Q. Xue, *"A Parallel-Strip Ring Power Divider With High Isolation and Arbitrary Power-Dividing Ratio,"* in IEEE Transactions on Microwave Theory and Techniques, vol. 55, no. 11, pp. 2419-2426, Nov. **2007**.

[9] K. Song, F. Xia, Y. Zhou, S. Guo and Y. Fan, *"Microstrip/Slotline-Coupling Substrate Integrated Waveguide Power Divider With High Output Isolation,"* in IEEE Microwave and Wireless Components Letters, vol. 29, no. 2, pp. 95-97, Feb. **2019.**

[10] L. Chiu, T. Y. Yum, Q. Xue and C. H. Chan, *"A wideband compact parallel-strip 180/spl deg/ Wilkinson power divider for push-pull circuitries,"* in IEEE Microwave and Wireless Components Letters, vol. 16, no. 1, pp. 49-51, Jan. **2006**.

[11] W. Liu, F. Wei, C. Pang and X. Shi, "*Design of a compact ultra-wideband power divider,"* 2012 International Conference on Microwave and Millimeter Wave Technology (ICMMT), Shenzhen, pp. 1-3, **2012**.

[12] M. C. Scardelletti, G. E. Ponchak and T. M. Weller, *"Miniaturized Wilkinson power dividers utilizing capacitive loading,"* in IEEE Microwave and Wireless Components Letters, vol. 12, no. 1, pp. 6-8, Jan. **2002**.

[13] B. Sutbas, E. Ozbay and A. Atalar, *"Compact and Wideband CPW Wilkinson Power Dividers for GaN MMIC Applications,"* 2018 48th European Microwave Conference (EuMC), Madrid, pp. 628-631, Nov. **2018**.

[14] Özipek, Ulaş. Design of an X-band GaN based microstrip MMIC power amplifier. Diss. Bilkent University, **2019**.

[15] Kavuştu, Muhammet. *S-band GaN high power amplifier design and implementation*. Diss. Bilkent University, **2019**.

[16] Rohde & Schwarz, "ZVA Vector Network Analyzer Specifications" ZVA datasheet, March **2014**.

[17] Pozar, D.M., "*Microwave Engineering"*, John Wiley and Sons, Inc., **1998**.

[18] Darwish, A.M., Ibrahim, A.A., Qiu, J., Viveiros, E., and Hung, H.A., "*Novel Ka-band 'offset-divider/combiner' with reflection cancellation"*, 2014 IEEE MTT-S International Microwave Symposium (IMS2014), pp. 1-3, **2014**.

[19] C. Li, L. B. Lok, A. Khalid, and D. R. Cumming, "*Coplanar ring divider with wideband high isolation performance*," Progress In Electromagnetics Research, vol. 25, pp. 1–10, **2011**.

[20] L. Chiu and Q. Xue, *"A parallel-strip ring power divider with high isolation and arbitrary power-dividing ratio,"* IEEE Transactions on Microwave Theory and Techniques, vol. 55, no. 11, pp. 2419–2426, **2007**.

[21] C. Li, L. B. Lok, A. Khalid, V. Papageorgiou, J. Grant, and D. R. Cumming, *"Millimeter wave coplanar stripline power dividers,"* International Journal of Microwave and Wireless Technologies, vol. 5, no. 3, pp. 205–212, **2013**.

[22] J. Jin, X. Lin, X. Gao, X. Zhuang, and Y. Fan, *"A dual-band power divider using parallel strip line with high isolation,"* Journal of Electromagnetic Waves and Applications, vol. 26, no. 11-12, pp. 1594–1601, **2012**.

[23] M. C. Scardelletti, G. E. Ponchak, and T. M. Weller, "*Miniaturized Wilkinson power dividers utilizing capacitive loading*," IEEE Microwave and Wireless Components Letters, vol. 12, no. 1, pp. 6–8, Jan **2002**.

[24] H. Yilmaz and M. Berroth, "*A dual-frequency Wilkinson power divider*," IEEE Transactions on Microwave Theory and Techniques, vol. 54, no. 1, pp. 278–284, Jan **2006**.

[25] E. J. Wilkinson, "*An n-way hybrid power divider*," IRE Transactions on Microwave Theory and Techniques, vol. 8, no. 1, pp. 116–118, Jan **1960**.

[26] M. Thorsell, M. Fagerlind, K. Andersson, N. Billstrom, and N. Rorsman,"*An x-band algan/gan mmic receiver front-end*,"IEEE Microwave and Wireless Components Letters, vol. 20, no. 1, pp. 55–57, Jan **2010**.

[27] A. Gurdal, U. Ozipek, B. Sutbas, and E. Ozbay, "*A high gain and high efficiency 15W X-band GaN power amplifier MMIC*," 2019 European Microwave Conference in Central Europe (EuMCE), Prague, May **2019**.

APPENDIX

APPENDIX 1 – Fabrication

APPENDIX 2 - Thesis Originality Report

APPENDIX 1 - Fabrication

X-band power divider/combiner structures in this thesis are designed by using the GaN MMIC process by Bilkent University Nanotechnology Research Center (NANOTAM). In this section, process steps for realized the passive components/circuits are explained with figures and SEM images. Example schematic view of the fabricated circuit is given in Figure 6.1.

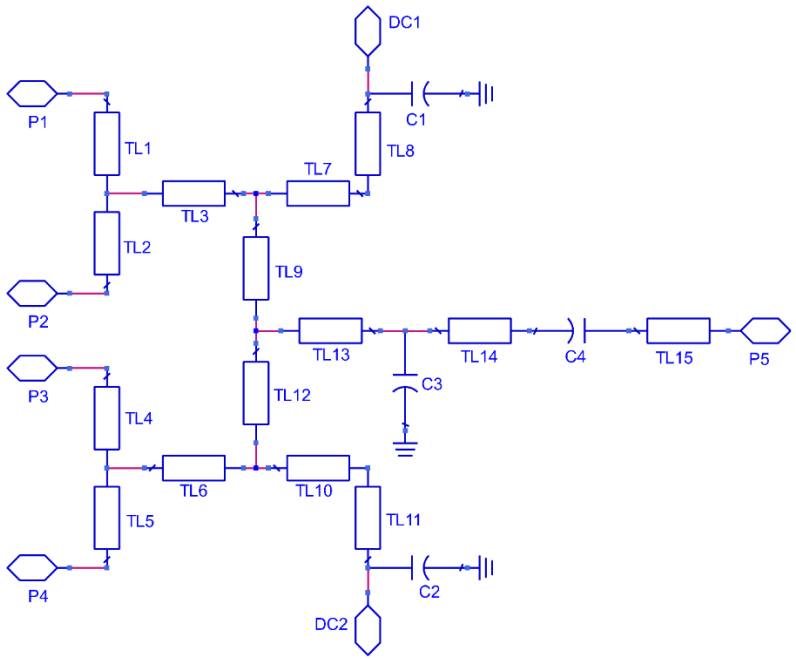


Figure 6.1 Example schematic view of the fabricated circuit

For the passive circuits/components, fabrication process starts with Thin Film Resistor (TFR) coating. By using RF magnetron sputter system, TaN TFR with 86nm thickness is deposited on SiC wafer that is 300um thickness shown in Figure 6.2.

Figure 6.2 Cross-section of wafer after TFR coating

Thereafter, Ti/Au metal stack is deposited using the electron beam evaporator system with thicknesses of 1um. This metal layer provides constituting the first metal layer of Metal-Insulator-Metal (MIM) capacitor and contact metal of the grounds and passive/active components of integrated circuits. Cross-section of wafer after Metal-1 coating is seen in Figure 6.3.

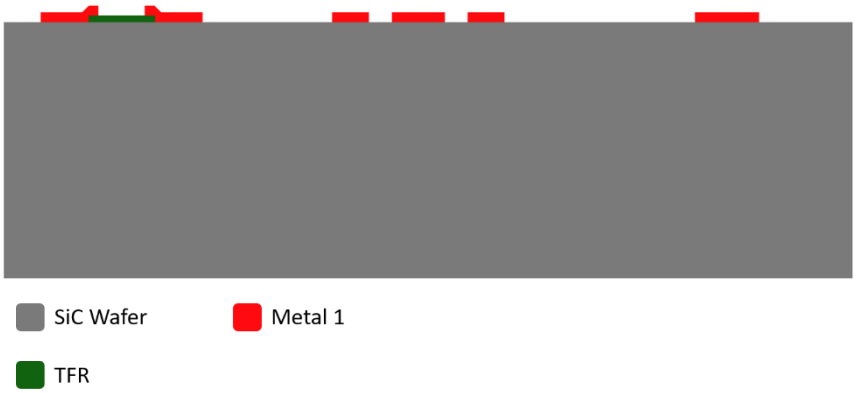


Figure 6.3 Cross-section of wafer after Metal-1 coating

Next step in fabrication, wafer is coated with a 300 nm-thick Si_3N_4 layer grown by Plasma-Enhanced Chemical Vapor Deposition (PECVD). This insulator is dielectric material of MIM capacitor and also used as passivation layer for active components (High-Electron-Mobility Transistor (HEMT)). Some areas on wafer are etched because of metal-metal connection. After etching photoresist layer (AZ5214) with AZ400K solution, dielectric passivation step is finished that is seen in Figure 6.4.

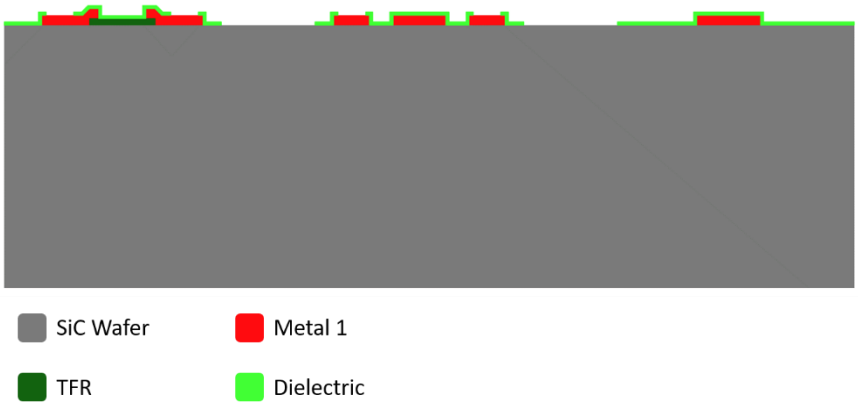


Figure 6.4 Cross-section of wafer after dielectric passivation step

Air-bridge resist is patterned as a sacrificial layer which the air-bridge was built on. Thickness of this layer is approximately 3um in order to reduce the parasitic effects and avoid short circuits at the metal-1 and metal-2 crossovers. Cross-section view of the wafer after formed air-bridge photoresist is shown in Figure 6.5.

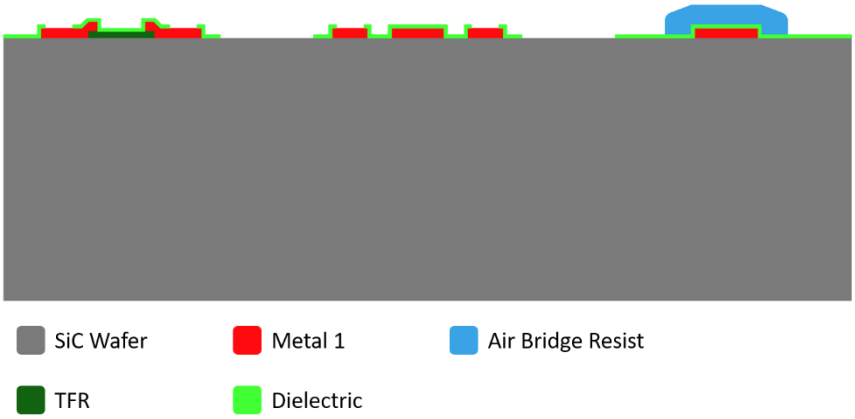


Figure 6.5 Cross-section of wafer after air-bridge resist is patterned

Ti/Au metal stack with 3µm total thickness is deposited as an interconnection by using e-beam evaporation. Au metal layer with a thickness of 4 µm is coated as an interconnection layer by using the electroplating system. After coating the interconnect metal layer, cross-section of the wafer is shown in Figure 6.6.

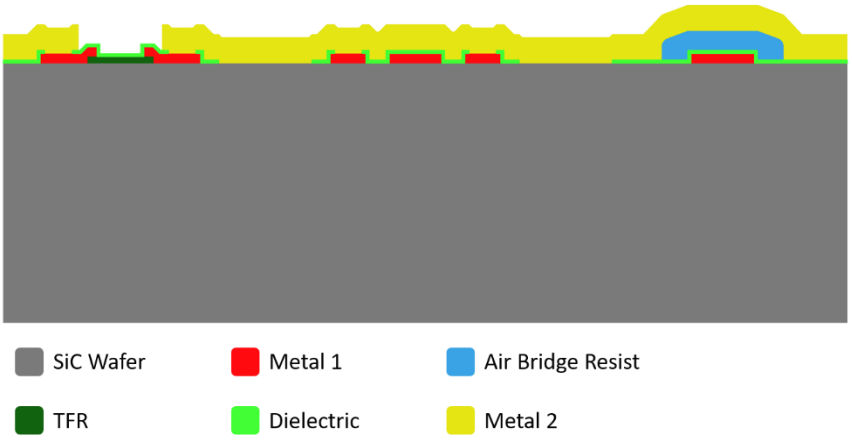


Figure 6.6 Cross-section of wafer after Metal-2 coating

After coating the interconnect metal, air bridge photoresist is cleaned by using AZ100 remover. The air bridge post structures were constituted for preventing any case of being short circuit of the metals by functioning as a jumper that is seen in Figure 6.7. In addition,

SEM image of the before and after bridge post cleaning step is shown in Figure 6.8. The front-side fabrication process is completed with this last step.

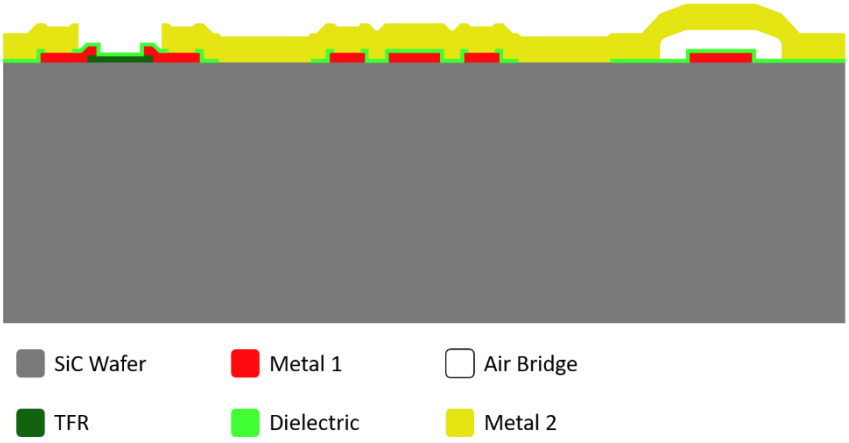
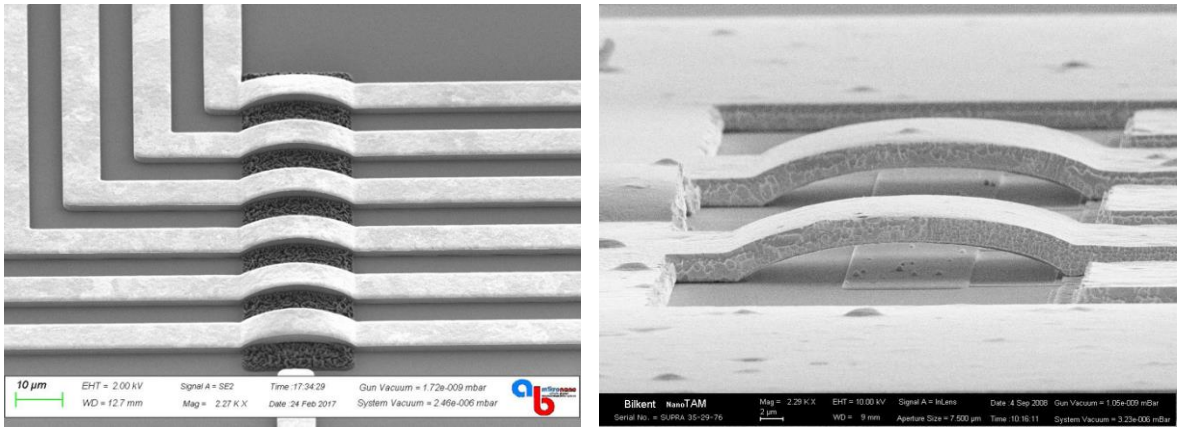


Figure 6.7 Cross-section of wafer after air-bridge resist etching



(a) (b)

Figure 6.8 SEM image of the air-bridge structure
(a) before bridge post cleaning (b) after bridge post cleaning

Back-side process starts with reducing wafer thickness. Sample is grinded down to 100 µm thickness using wafer grinder system (Figure 6.9).

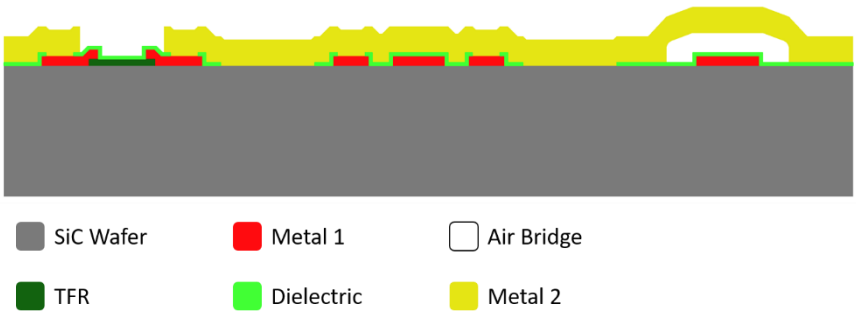


Figure 6.9 Cross-section of wafer after back grinding of wafer

Thereafter, back-via holes are formed by using ICP-RIE dry etching that is shown in Figure 6.10. Radius of the via-holes are 84nm with 83^0 sidewall angle. SEM image of the via-hole profile is shown in Figure 6.11.

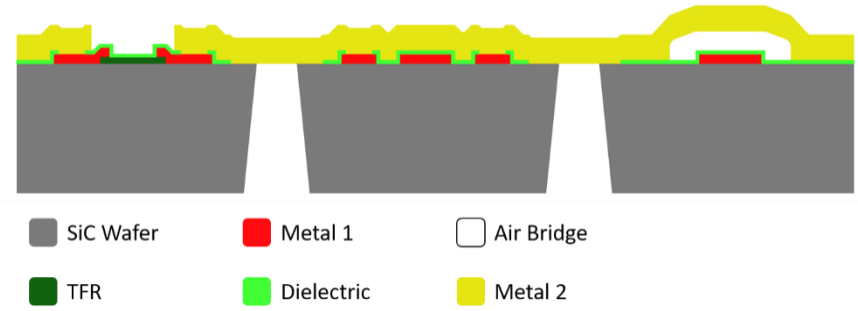


Figure 6.10 Cross-section of wafer after via etch process

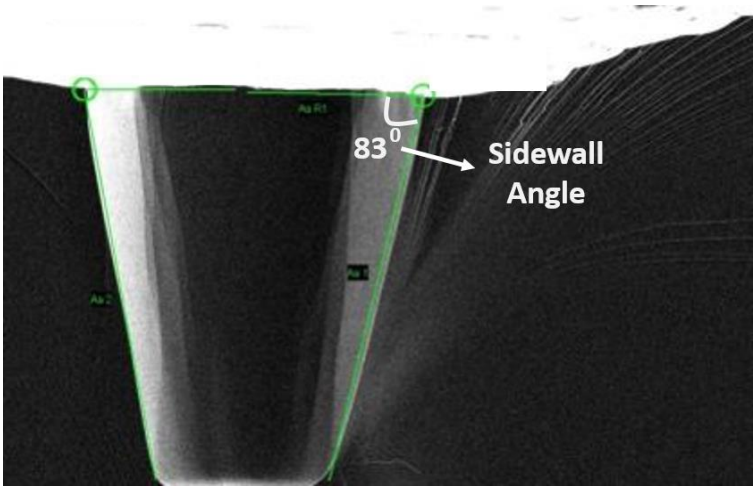


Figure 6.11 Cross-sectional SEM image of Via-hole

Au metal layer with a thickness of 4 μm is coated inside the via-holes on the back side of the wafer by using the electroplating system. Therefore, connection of front and backside is

provided by this metallization. Back-Side process is finished after the back-metallization step. Final cross section of wafer is shown in Figure 6.12.

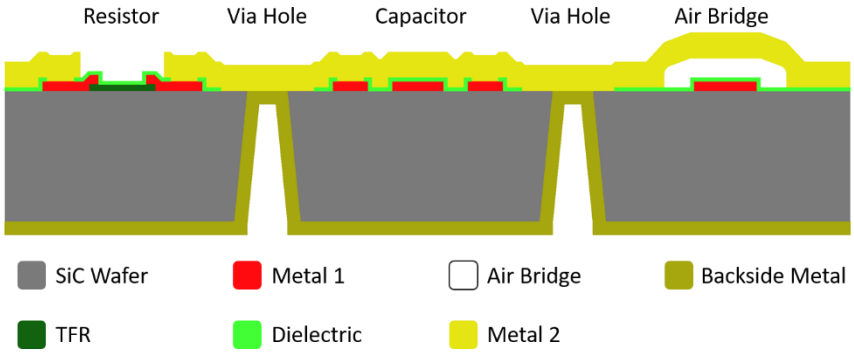


Figure 6.12 Cross-section of wafer after back-side metallization

In this thesis work, process steps are given for constructing passive components/circuits. The whole process in NANOTAM is given in [14] and [15] thesis works. Cross section of wafer for whole process is given in Figure 6.13 [14].

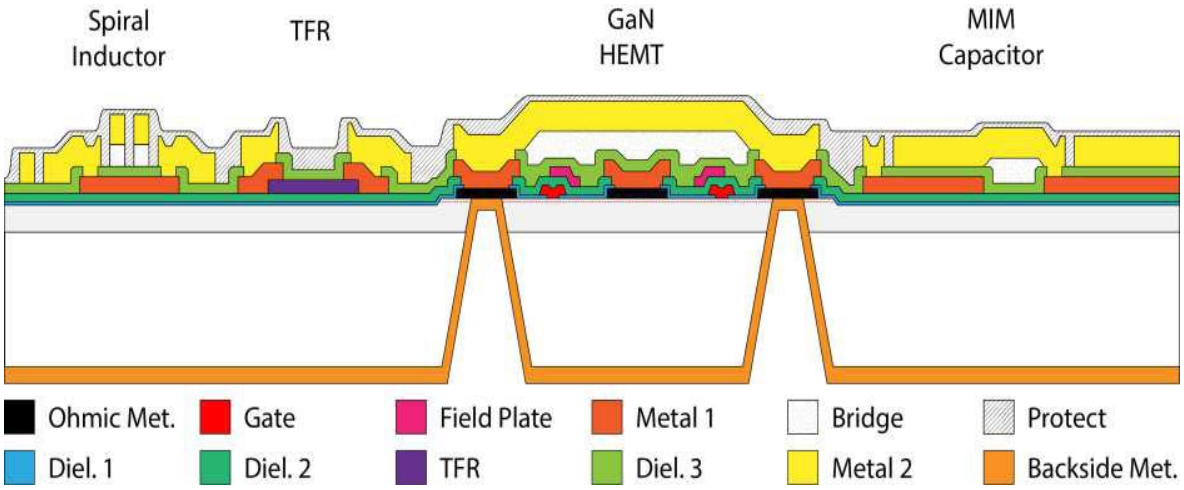
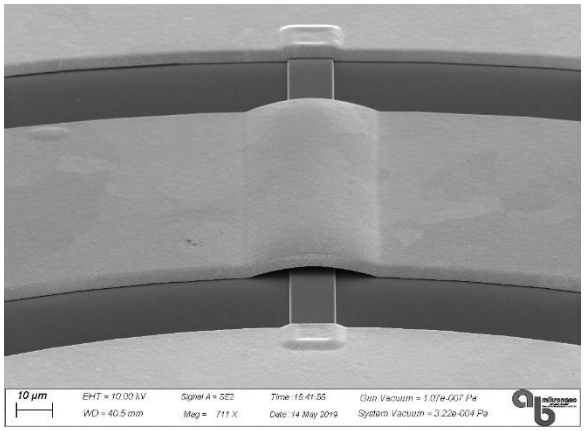
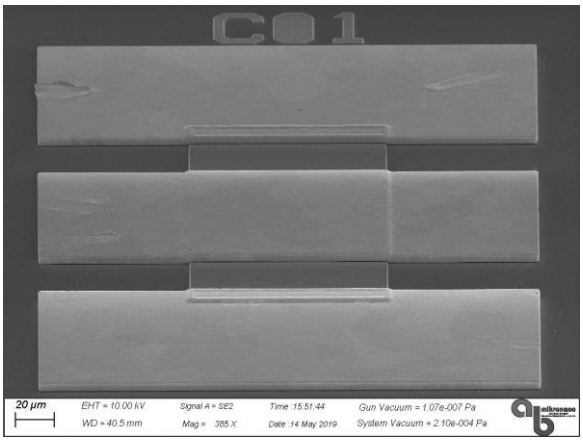


Figure 6.13 Cross-section of wafer for whole process

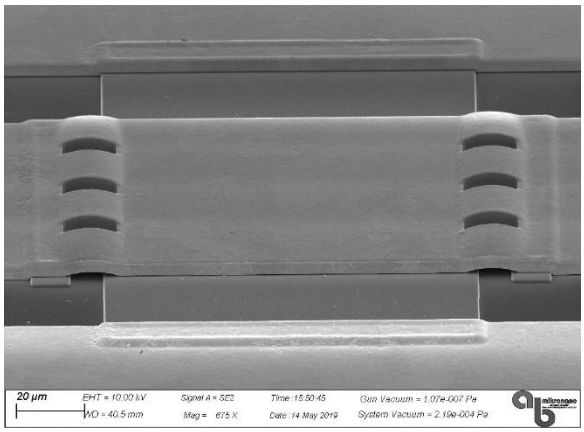
In addition, SEM image of some fabricated lumped components are given below Figure 6.14.



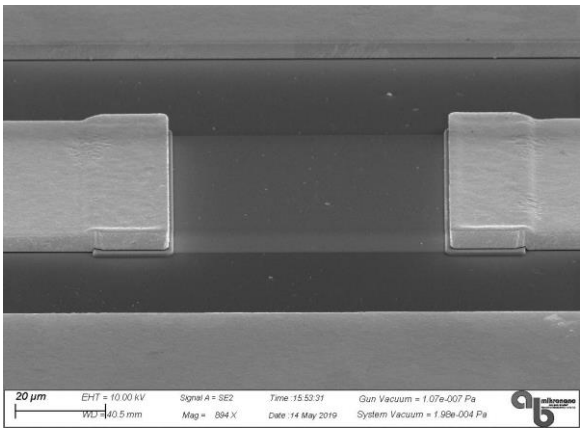
(a)



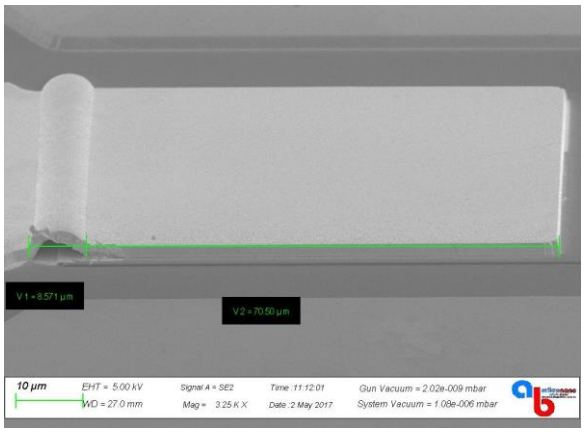
(b)



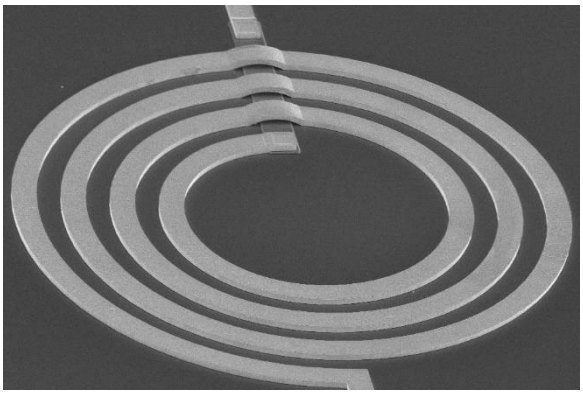
(c)



(d)



(e)



(f)

Figure 6.14 SEM image of the (a) Air-bridge (b) Shunt capacitor (c) Shunt capacitor with air-bridge (d) Thin film resistor (e) Series capacitor (f) Inductor

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